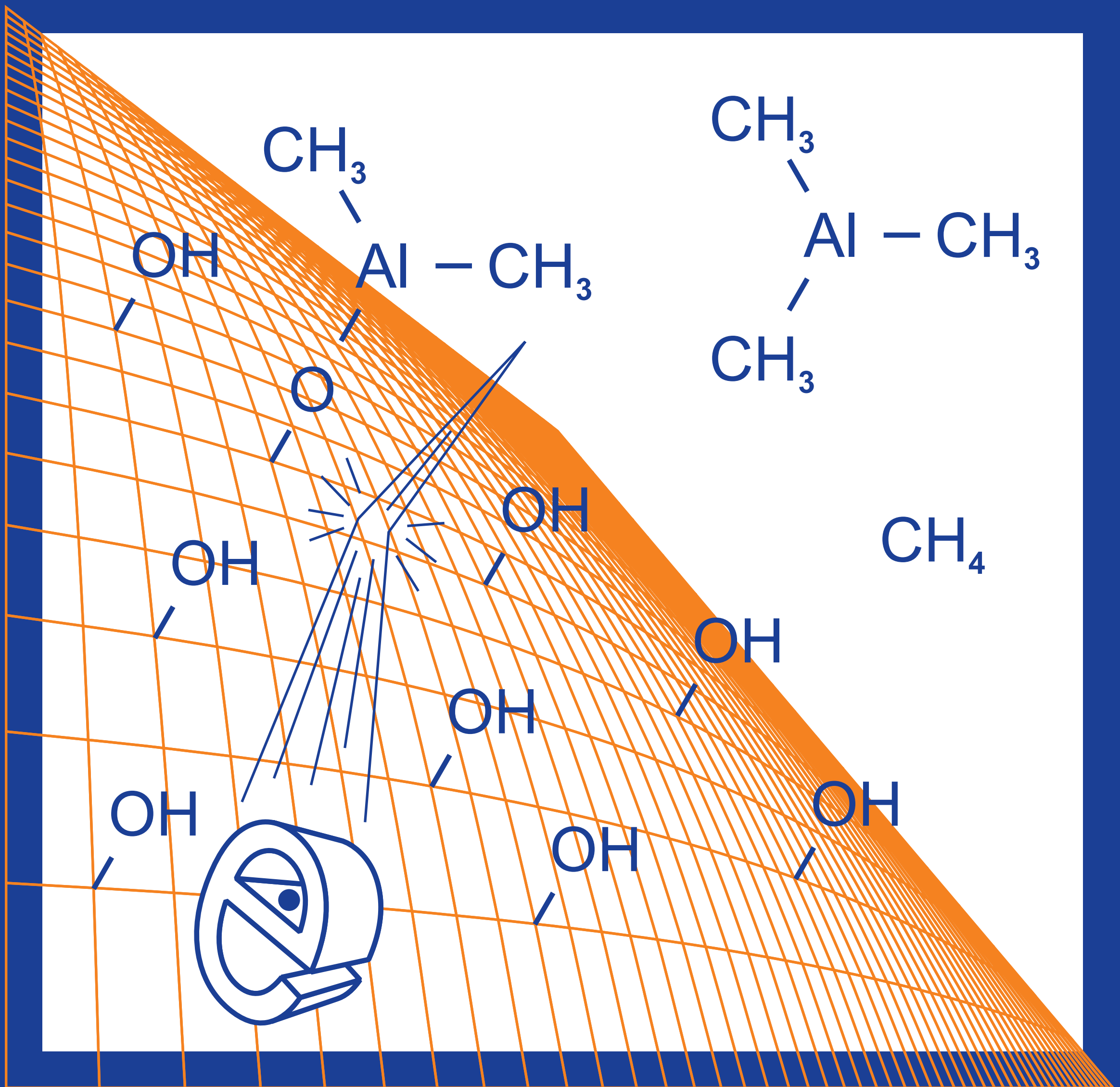
In-situ RHEED and characterization of ALD Al_2O_3 gate dielectrics



Radko Bankras

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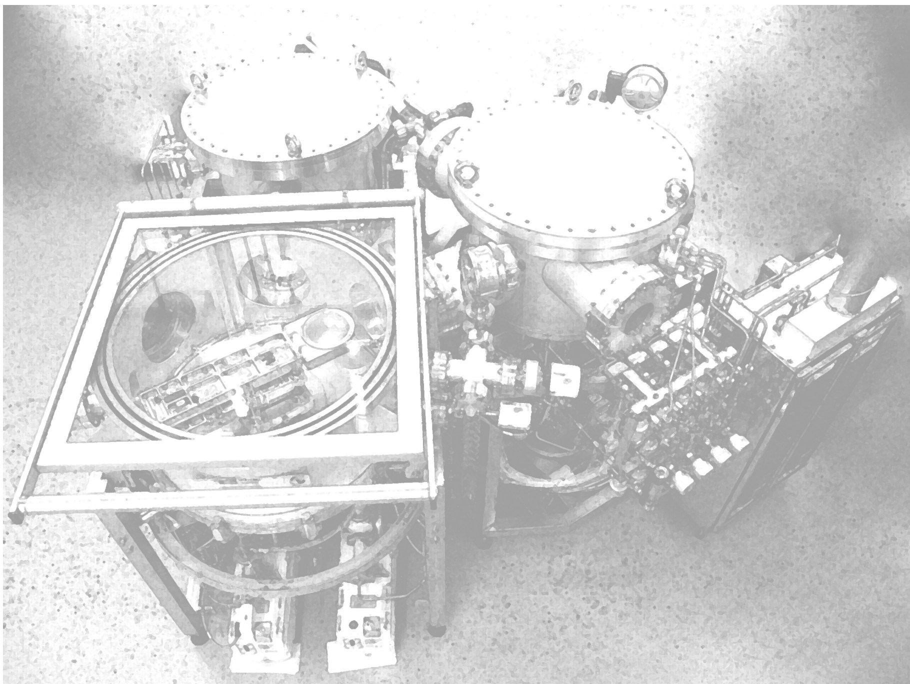

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In-situ RHEED and characterization of ALD Al_2O_3 gate dielectrics

DISSERTATION

to obtain
the doctor's degree at the University of Twente,
on the authority of the rector magnificus,
prof.dr. W.H.M. Zijm,
on account of the decision of the graduation committee,
to be publicly defended
on Wednesday, November 1st 2006 at 13:15

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This dissertation is approved by
the promoter prof.dr. J. Schmitz and
the assistant promoter dr. J. Holleman.

To my parents, Jacques and Mia Bankras,
for their support and encouragement.

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Introduction

The books used in the (electrical) engineering curriculum usually have titles that start with "Introduction to ..." or "First principles of ...". This observation is easily followed by a question about the use of books on matter of importance. However, after graduation the student is deployed in the experimental field of the unknown and not-yet-known. Progress in engineering has led to some fundamental boundaries of basic principles. The infinite urge of scientific progress now requires solutions, which can not (yet) be found in textbooks.

The introduction of personal computers in the late seventies and early eighties of the twentieth century can be seen as the start of the digital era for consumers. For several years, the massive electronic calculators could only be afforded and operated by large companies and universities. [0.1] The ability to perform vast amounts of effortless calculations is attributed to the invention of the transistor in 1947 by W.B. Shockley, J. Bardeen and W.H. Brattain. [0.2] The novel solid state electronic switch was eventually developed into the first MOSFET, or metal oxide semiconductor field effect transistor. Nowadays, the MOSFET still forms the basis of most products of the multibillion dollar semiconductor industry.

The success of the semiconductor industry has been its ability to engineer single transistors into ever more complex integrated circuits. [0.3] Manufacturing highly valued products from a minimum amount of material, drove the development of advanced semiconductor technologies. The downscaling trend

of semiconductors is a balancing act, in which expensive new technologies have to be approved by additional profit from being able to manufacture more products per wafer. “Last year, more transistors were produced - and at lower cost - than grains of rice”. [0.4] However, after five decades of downscaling, some fundamental limits have been reached.

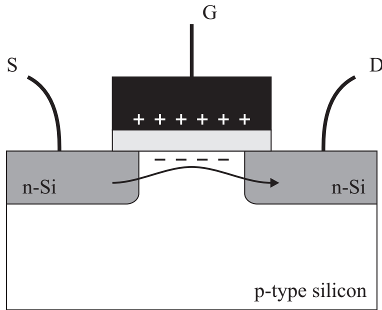

Figure 1: schematic cross-section of a field effect transistor, with source (S), gate (G) and drain (D) connections. The gate oxide is light gray colored and isolates the gate (black) from the silicon substrate.

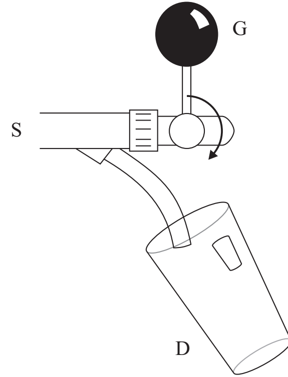

Figure 2: analogue of a MOSFET transistor: the flow from source to drain is controlled by a gate, which for the best result should only be positioned in fully opened (or closed) state.

The field effect transistor can be opened (or closed) due to a counter charge of the gate potential in the semiconductor. The amount of charge depends on the applied gate bias and the dielectric properties of the isolation material between gate and substrate. This gate oxide has followed the downscaling trend up to thicknesses of only a few atomic layers. Unfortunately, leakage currents through the gate oxide have increased exponentially with the reduction of oxide thickness and have now become unacceptable.

The aim of the research, as presented in this dissertation, is to contribute to the development of a replacement gate dielectric. The approach was to study the initial growth of high-κ metal oxides in an ultra-clean (high vacuum) atomic layer deposition technology by in-situ characterization. One of the most studied high-κ dielectric materials is aluminum oxide and is often used as example material for gate oxide replacement. Hence the title of this dissertation “In-situ RHEED and characterization of ALD Al_2O_3 gate dielectrics”.

In chapter 1 all relevant aspects of gate dielectrics will be discussed. The information provided in this chapter should form a base for the experimental work on pulsed laser deposition (PLD) and atomic layer deposition (ALD), as presented in chapters 2 and 3, respectively. Both deposition techniques have been used to deposit Al_2O_3 gate dielectrics. Chapter 4 discusses the use of an in-situ characterization technique in an atomic layer deposition reactor, which is commonly used in pulsed laser deposition systems: reflection high-energy electron diffraction (RHEED). The chapter presents the implementation of the RHEED technique in the ALD reactor and the results obtained from measurements during Al_2O_3 deposition. The results from modeling RHEED during ALD growth, used to interpret the results obtained in chapter 4, will be discussed in chapter 5. Chapter 6 presents the high frequency electrical characterization of Al_2O_3 gate dielectrics in a special test structure. Finally, a summary of results, the conclusions of this dissertation, the original contributions of this work and recommendations for further research can all be found in chapter 7.

This project has been a collaboration between the chairs of Semiconductor Components and Solid State Physics of the University of Twente. The project was supported by Dutch Technology Foundation STW (TMF5379, "High-κ dielectric material for MOS gate dielectrics"). The users' committee consisted of Philips Research and ASM International representatives.

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Part I

Background

1 Gate dielectrics

The use of integrated circuits (or chips) has increased for several decades at an incredible rate. Nowadays almost every household appliance is digitally controlled and contains functionality beyond the grasp of most users. However, the customer still demands electronic devices to be smaller, operate faster, have increased capabilities, be more reliable and use less energy. In order to answer to the customer's requests, (or actually to be able to satisfy the customer with a new product before industrial competitors advance), circuit designers have been taking advantage of every bit of improvement in the integrated circuit technology.

1.1 Technology development

Since the first use of metal oxide semiconductor (MOS) transistors in the early 1960s, the manufacturing process has been improved up to a highly advanced semiconductor technology. The ability to scale transistors to decreasing dimensions has resulted in higher performances and made CMOS architecture the dominant technology in current integrated circuits. This downscaling trend, as described by Moore's law, has reduced MOS gate dimensions from 10 µm in 1970 to a present day size of less than 0.1 µm.

For decades silicon dioxide has been used as the gate dielectric material for standard MOS technology. One of the problems with scaling MOSFETs beyond the 0.1 µm technology, is the increasing leakage current through the gate dielectric. The traditional SiO_2 gate dielectric will reach fundamental scaling limits near the effective electrical thickness of only a few molecular

layers. The International Technology Roadmap for Semiconductors (ITRS) indicates that the rate of device scaling would produce 45 nm generation devices using equivalent gate oxide thicknesses (EOT) of 0.7 nm in 2010 (see table 1.1). To enable MOS scaling in the future, solutions will have to be found and the semiconductor technology will have to be altered.

year	DRAM ½ pitch [nm]	physical equivalent oxide thickness [nm]
2000*	165	1.9-2.5
2002*	130	1.5-1.9
2004	90	1.2
2006	70	1.0
2007	65	0.9
2008	57	0.8
2010	45	0.7
2013	32	0.6
2016	22	0.5
2018**	18	0.5
2020**	14	0.5

Table 1.1: technology development in ITRS editions [1.1] of 1999/2000(*), 2003/2004 and 2005(**), displayed as DRAM ½ pitch design dimensions and physical equivalent oxide thickness of transistors in microprocessor units.

1.2 High dielectric constant materials

The typical leakage current of SiO_2, at a gate bias of 1 V, changes from 10^{-12} A/cm^2 at 3.5 nm to 10 A/cm^2 at 1.5 nm. [1.2] The leakage current density of future generation CMOS devices is forecast to exceed 1 kA/cm^2. [1.1] For use in low-power applications, the leakage current of the gate dielectric has to be less than 10^{-3} A/cm^2. [1.3] A solution could be found in replacement of the traditional thermally grown silicon dioxide, by deposition of an alternative material with a higher relative permittivity (κ). However, this will only (temporarily) solve one of the barriers that are limiting future development of the CMOS technology. Related to the search for a suitable high-κ dielectric material are the research of different starting materials (substrates), low-κ materials for interconnect dielectrics and alternative gate electrode metals. The question is for how long an advanced technology can be improved and when the semiconductor industry starts the development of new technologies to replace CMOS technology.

1.2.1 Polarizability and (relative) permittivity

In order to determine which dielectric materials are suitable for high-κ gate oxide application, a detailed understanding is required of how different materials affect an electric field. The electric field is formed between two isolated metal plates (the gate and the substrate) with a potential difference, e.g. when a positive charge is applied to the gate. This electric field is directed from the positively charged plate to the negatively countercharged plate as drawn in figure 1.1 and is given by

$$E = \frac{Q}{\varepsilon_0 \cdot d}, \tag{1.1}$$

where Q is the charge per unit area on a plate, d the distance between the plates and ε_0 the permittivity of free space.

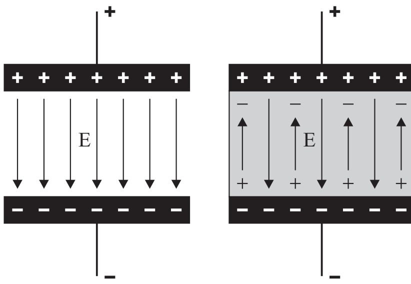

Figure 1.1: electric field between two charged metal plates in free space and in a dielectric material.

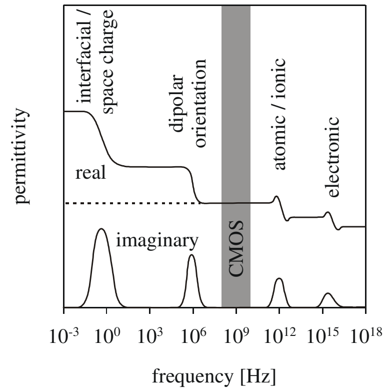

Figure 1.2: frequency dependence of the real ε' and imaginary ε'' parts of the dielectric permittivity. [1.4]

When the medium between the two metal plates is a polarizable dielectric material, the electric field is reduced by an internal counterfield. This internal electric field is the result of the interaction between the applied charges and bound charges in the dielectric material. A negative charge is attracted (displaced) towards the positive plate and vice verse. The orientation of (polarization) charges in the dielectric material is possible by different polarization mechanisms of the material. The actual electric field is the sum (subtraction)

of both electric fields and is calculated by

$$E = \frac{Q}{\kappa \cdot \varepsilon_0 \cdot d}. \quad (1.2)$$

The permittivity of a material is a measure of the interaction between an electric field and the material. Equation 1.3 [1.5] shows the relation between displacement $\boldsymbol{D}$, electric field $\boldsymbol{E}$ and polarization $\boldsymbol{P}$

$$\boldsymbol{D} = \varepsilon_0 \cdot \boldsymbol{E} + \boldsymbol{P} = \varepsilon_0 \cdot (1 + \chi_e) \cdot \boldsymbol{E} = \kappa \cdot \varepsilon_0 \cdot \boldsymbol{E}, \quad (1.3)$$

in which χ_e is the electronic susceptibility of the material. The commonly used term dielectric constant is the permittivity of a material, normalized to the permittivity of free space ε_0. A list of symbols used in this dissertation can be found on page 165.

Figure 1.2 shows how the different polarization mechanisms, that make up the permittivity of the material, are lost at elevated frequencies of the applied external bias. Electronic polarization is a shift of the electron cloud of an atom from its center position. The average distance between the negative electron cloud and positive nucleus forms a small electric field. Atomic or ionic polarization (distortion polarization) is the displacement of the negatively charged cations and positively charged anions that form the molecule. [1.6] A third contributing component is orientational polarization by alignment of permanent dipolar molecules. In principle all components can contribute to formation of a steady state internal electric field. Thus, the dielectric constant of a material depends on the frequency of the applied potential difference. Some polarization mechanisms (e.g. dipolar orientation) may be very weak or not present at all in the dielectric material, as visualized by the dashed line in figure 1.2. The imaginary part of the complex permittivity is the dielectric loss due to out-of-phase polarization and ohmic loss due to free charge carriers in the dielectric. The loss tangent $\tan(\delta)$ is the ratio between imaginary ε'' and real ε' parts of the permittivity and therefore one measure for the dielectric quality of a material

$$\tan(\delta) = \frac{\varepsilon''}{\varepsilon'} \ll 1. \quad (1.4)$$

In the frequency range of CMOS applications, 100 MHz - 10 GHz, only atomic/ionic and electronic polarization are able to contribute to the permittivity. The frequency dependence of the dielectric constant is often omitted in publications. The relation of the relative permittivity as squared refractive index, is only valid at optical frequencies. The dielectric constant at CMOS frequencies is higher, due to the contribution of atomic polarization.

1.2.2 Charge tunneling mechanisms

Thus, permittivity is an indication of the electrical charge a material is able to store. A material with higher permittivity is able to store more charge than a material with lower permittivity. The amount of charge is limited by the dielectric strength, which is the maximum electric field the dielectric material can withstand without breakdown. [1.5] Dielectric breakdown occurs when electrons are pulled from the molecules due to the large electric field. The free electrons accelerate and collide with other atoms. The result is an avalanche effect of ionization (due to collisions), the creation of permanent dislocations and possibly a conducting path between gate and substrate.

At lower electric fields, charge transport between the gate and the substrate is still possible and not even necessarily destructive or a reliability issue. The isolating properties of a dielectric material are the result of the relatively large (but not infinite) energy bandgap. The energy bandgap is the energy required to change an electron from a nonconducting (bound) state to a conducting (free) state. More important is the alignment of the energy bandgap to the energy levels of charge carriers in adjacent materials.

For electron transport from the semiconductor to the gate, the barrier height is the conduction band offset ΔE_{C}. The barrier height for electrons from the metal gate, Φ_{B}, is defined as the difference between the Fermi level in the gate and the conduction band level of the dielectric. The difference between both barriers is the electron affinity of the substrate χ and the metal workfunction Φ_{M} of the gate

$$\Delta E_{\mathrm{C}} = q \cdot (\chi + \Phi_{\mathrm{B}} - \Phi_{\mathrm{M}})\,. \tag{1.5}$$

Figure 1.3 shows the energy bandgaps and their offsets with respect to a silicon substrate, of several high-κ materials and silicon oxide. Aluminum oxide has only a dielectric constant of about 9, but also the highest bandgap of all high-κ materials. Ludeke [1.8] obtained an Al_2O_3/Si conduction band offset of ΔE_{C} = 2.78 eV. Obviously, the barrier height and energy bandgap should be included in the selection of a new dielectric material.

Several mechanisms enable electrons to overcome the energy barrier of the dielectric, either by gaining sufficient energy or by lowering of the energy barrier. Electrons gain energy from for example thermal excitation (phonons) or in an electric field. The required energy is reduced by intermediate energy trap levels (caused by defects in the dielectric) or an applied electric field, resulting in an effective lowering of the energy barrier. The so-called Frenkel-Poole emission is the field-enhanced electron emission from a trap level to the

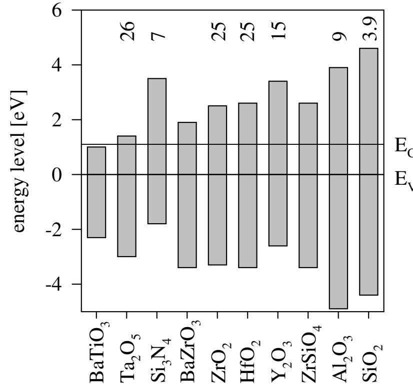

Figure 1.3: bandgap offset of different high-κ dielectrics, with respect to the conduction band and valence band energy levels of the silicon substrate. [1.7] The dielectric constant is displayed at the top of the bar.

lowered conduction band level. Although numerous other charge tunneling mechanisms have been published [1.9], the Fowler-Nordheim, Frenkel-Poole and direct tunneling mechanisms are most commonly used to describe leakage currents.

Under sufficiently high electric fields, electrons can tunnel through a very thin dielectric layer by the Fowler-Nordheim tunneling mechanism. The increase in Fermi level in the gate, changes the barrier height of the oxide to a triangular shape (see figure 1.4). The reduction of the effective oxide thickness results in the Fowler-Nordheim tunneling current density

$$I_{\mathrm{FN}} = A \cdot {E_{\mathrm{ox}}}^2 \cdot \exp\left(\frac{-B}{E_{\mathrm{ox}}}\right), \tag{1.6}$$

with

$$\begin{aligned} A &= \frac{q^3}{8\pi \cdot h \cdot \Phi_{\mathrm{B}} \cdot m^*}, \\ B &= \frac{8\pi}{3q \cdot h}\sqrt{2m^* \cdot m \cdot {\Phi_{\mathrm{B}}}^3}, \end{aligned}$$

where m^* is the relative effective mass of electrons in the dielectric. [1.10] The value and description of the other symbols can be found in the table on page 165.

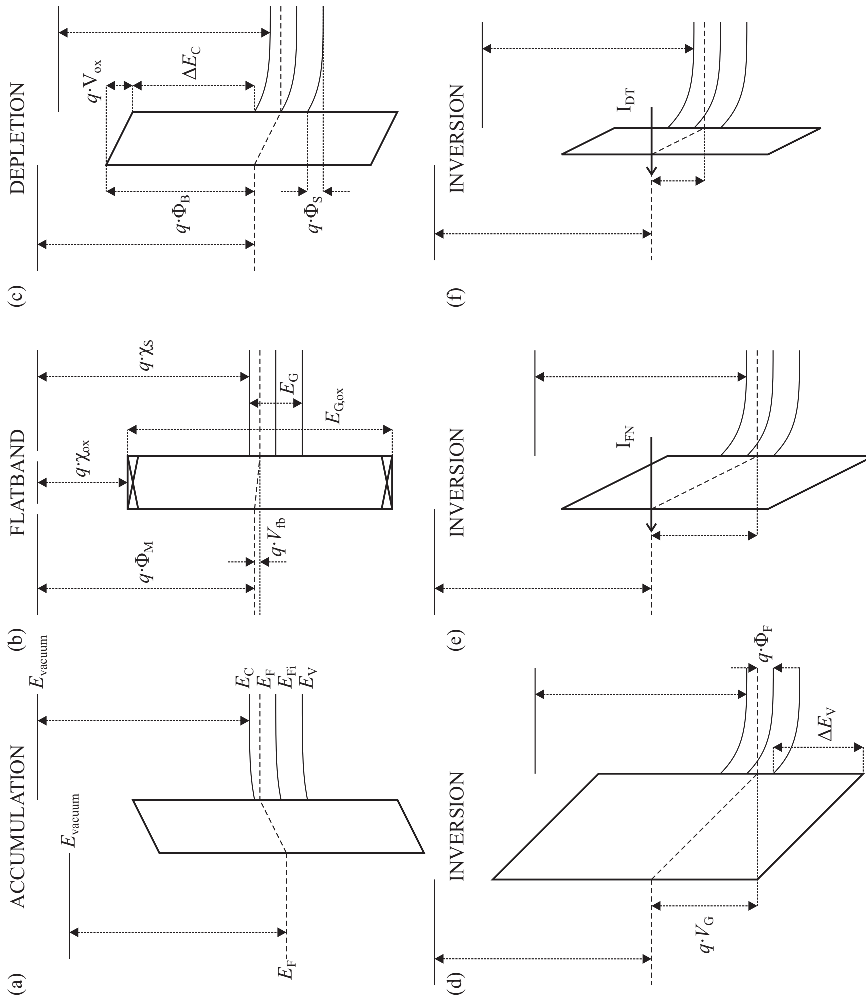

Figure 1.4: energy band diagrams of a metal oxide stack on n-type silicon: (a) accumulation, (b) flatband conditions, (c) depletion, (d) inversion (thick oxides), (e) inversion (Fowler-Nordheim tunneling) and (f) inversion (direct tunneling).

Electrons can also tunnel directly through the full oxide thickness of thin dielectric layers. The direct tunneling mechanism dominates at low gate voltages in thin dielectric layers. The current density of the direct tunneling process is (in strong accumulation) approximately [1.11]

$$I_{\mathrm{DT}} = \frac{A \cdot E_{\mathrm{ox}}^{2}}{\left(1-\sqrt{1-\frac{q \cdot V_{\mathrm{ox}}}{\Phi_{\mathrm{B}}}}\right)^{2}} \cdot \exp\left(\frac{-B}{E_{\mathrm{ox}}} \cdot \left[1-\left(1-\frac{q \cdot V_{\mathrm{ox}}}{\Phi_{\mathrm{B}}}\right)^{3/2}\right]\right). \quad (1.7)$$

Figures 1.5 and 1.6 show the calculated tunneling current densities according to the direct and Fowler-Nordheim mechanisms (equations 1.6 and 1.7), for 0.8 - 1.4 nm SiO_2 and Al_2O_3, respectively.

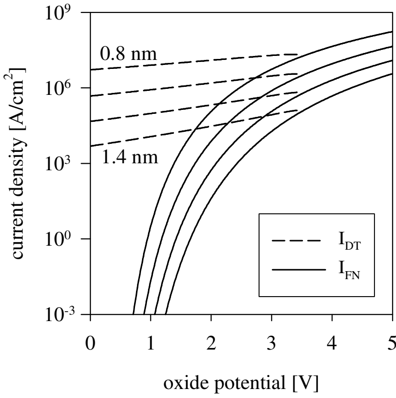

Figure 1.5: direct and Fowler-Nordheim tunneling current densities in 0.8 nm, 1.0 nm, 1.2 nm and 1.4 nm SiO_2, with barrier height Φ_B = 3.5 eV and relative effective electron mass m* = 0.26.

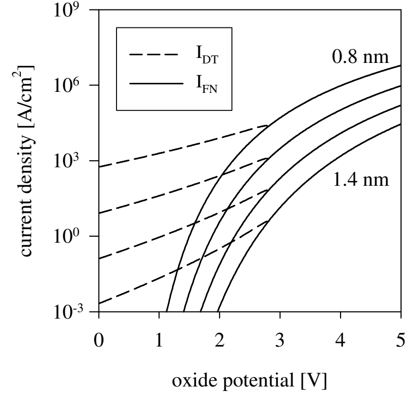

Figure 1.6: tunneling current densities in 0.8 nm, 1.0 nm, 1.2 nm and 1.4 nm equivalent oxide thickness Al_2O_3, with barrier height Φ_B = 2.8 eV and relative effective electron mass m* = 0.23.

The interface of silicon substrate and gate dielectric usually consists of a mixture of both materials or sometimes even a different material. A material with different properties can also be present at the interface between gate dielectric and gate electrode. The dielectric layer therefore actually consists of up to three capacitors in series

$$\frac{1}{C_{\text{dielectric stack}}} = \frac{1}{C_{\text{lower interface}}} + \frac{1}{C_{\text{bulk oxide}}} + \frac{1}{C_{\text{upper interface}}}. \quad (1.8)$$

This stack of dielectric materials could be engineered to have a high dielectric constant bulk and a high barrier height at the interface to reduce charge tunneling. Advanced gate stack engineering could lead towards laminated structures of different dielectric materials.

1.2.3 Downscaling gate dielectrics

The higher dielectric constant of a new gate oxide will allow the use of a physically thicker layer, without a reduction in the gate capacitance. The gate capacitance is a measure of the required charge (supply voltage) to open the transistor, and is calculated as

$$C_{\mathrm{ox}} = \frac{\kappa \cdot \varepsilon_0 \cdot A}{t_{\mathrm{ox}}}. \tag{1.9}$$

Table 1.2 shows how the different MOSFET parameters can be scaled for a transistor with smaller footprint and similar characteristics. Although the scaling according to this constant electric field principle results in a constant power dissipation density and constant drain current per channel width I_{d}/W, the proportional reduction in applied bias and threshold voltage is not desirable. The tradeoff between performance (speed) and power may result in selectively scaling some parameters less rapidly. [1.12]

parameter		scaling factor
device dimensions	$t_{\mathrm{ox}}, L, W, x_{\mathrm{j}}$	$1/\alpha$
area	A	$1/\alpha^2$
doping concentration	N_{A}	α
applied bias	$V_{\mathrm{ds}}, V_{\mathrm{g}}, V_{\mathrm{sub}}$	$1/\alpha$
current	I_{d}	$1/\alpha$
threshold voltage	V_{t}	$1/\alpha$
gate capacitance	C_{ox}	$1/\alpha$

Table 1.2: constant electric field scaling factors of MOSFETs. [1.13]

The downscaling of the lateral dimensions of the MOSFET by a factor α, requires scaling of the oxide thickness by the same factor. Simplified, the scaling of lateral dimensions is limited by photolithography capabilities. Scaling of the oxide thickness, however, is limited by allowed power consumption due to the leakage current through the oxide. Especially when the applied bias is reduced by a smaller factor than the oxide thickness, the limitations of the gate

insulator are approached. Equation 1.9 shows that the dielectric constant is the only device parameter, which can compensate for the reduced oxide thickness.

The gate voltage applied to a MOS structure can be described by

$$V_G = V_{fb} + \Phi_S + V_{ox} = V_{fb} + \Phi_S - \frac{Q}{C_{ox}}, \tag{1.10}$$

where Q is the (gate bias induced) substrate charge per unit area. [1.10] The ratio of substrate charge and oxide capacitance is the potential difference responsible for the substrate charge. The flatband voltage V_{fb} and surface potential Φ_S are gate voltage components, required to balance the intrinsic charge in the semiconductor and the potential drop in the substrate, respectively.

The properties of different dielectric materials are commonly presented in relation to their equivalent oxide thickness (EOT), or capacitance equivalent thickness (CET). This normalized parameter is the thickness of a silicon dioxide layer, required to achieve the same gate capacitance. Some publications differentiate between the two parameters, e.g. the CET as extracted from the measured accumulation capacitance, the EOT as effective thickness after compensation for parasitic effects (quantum mechanical, gate depletion, etc.). The method of equivalent thickness determination is, therefore, of importance when comparing results. The EOT is basically calculated as

$$EOT = \frac{\kappa_{SiO_2}}{\kappa_{ox}} \cdot t_{ox}, \tag{1.11}$$

in which the dielectric constant of SiO_2 is 3.9. A physically thicker layer of high-κ material (a dielectric constant exceeding that of SiO_2) is used for the same EOT value, compared to a silicon oxide layer. The equivalent oxide thickness of a new dielectric material is expected to become less than 1.0 nm in 2007 (see table 1.1).

Figure 1.7 shows that the selection of a new dielectric material can not be based on only its dielectric constant. The general trend shows that the permittivity is related to the reciprocal of the energy bandgap. Although the presented permittivity data ε_∞ is based on the refractive index, the additional ionic polarization component is not expected to invalidate the trend.

1.2.4 Qualification for process integration

Three types of dielectric materials (for MOS applications) can be found in literature: ferroelectric materials, polymers and metal oxides (incl. silicon

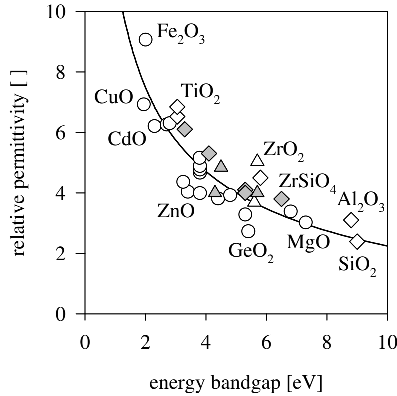

Figure 1.7: correlation between relative permittivity ε_∞ and energy bandgap E_G. Source of permittivity data: open [1.14] and closed [1.7] symbols; energy bandgap data: circle [1.14], diamond [1.7] and triangle [1.15]. The line represents the relation as proposed by Duffy [1.16].

oxinitrides). The first group contains (Pb,Zr)TiO_3 (PZT), $SrBi_2Ta_2O_9$ (SBT) and (Ba,Sr)TiO_3 (BST), which are materials with a very high dielectric constant (κ = 300 … 800). Currently, these dielectrics are used in high density DRAM capacitors and nonvolatile ferroelectric RAM (FRAM). In the latter, the extremely high (semi permanent) polarization of the material is used to store data. The relatively new field of organic electronics has gained interest in dielectric polymer materials, but these will be left out of consideration for gate dielectric replacement here, due to its incompatibility with (standard) semiconductor technology. Note, some low-κ dielectrics used for interconnect isolation are organic. Metal oxides have lower dielectric constants than the ferroelectric materials, but several are still higher than silicon dioxide.

A fourth group of dielectrics should be mentioned to included special dielectrics, e.g. air, pure water, vacuum and certain gases. Obviously, these dielectrics are not suitable for integration as gate dielectric in integrated circuits. A more appropriate classification scheme for dielectric materials is their dielectric constant. Table 1.3 shows the typical division of the range of dielectric constants. The search for a suitable gate oxide replacement is focused at materials in the third group with a dielectric constant of about 20.

The qualification of a new high-κ dielectric is not limited to a suitable dielectric constant and acceptable barrier height for charge tunneling. Requirements of conduction- and valence band offsets are closely related to the energy

	dielectric constant	classification	example(s)
1	$\kappa < 3.9$	low-κ	SiLK, TEOS, MSQ
2	$3.9 \leq \kappa < 10$	medium-κ	Si_3N_4, Al_2O_3, HfSiON
3	$10 \leq \kappa < 100$	high-κ	HfO_2, Ta_2O_5
4	$100 \leq \kappa$	super-high-κ	PZT, SBT, BST

Table 1.3: classification scheme of dielectric materials.

level of charge in the gate electrode and substrate. It is not unthinkable to engineer a CMOS process with different gate stacks (oxide and gate metal) for NMOS and PMOS transistors. The dielectric material should also have a high breakdown voltage to withstand the large electric fields. Imperfections in the oxide and near the interfaces easily affect the operation of the transistor. Built-in charge, interface trap density and channel mobility are important parameters for the dielectric quality of the oxide.

Implementation of a new material requires at least a good adhesion to the other process materials, mainly the silicon substrate and gate material. The thermal stability of the material (in contact with other materials) is of interest. This material property indicates if high temperature process steps during and after deposition of the dielectric, result in interface layer formation, diffusion, crystallization, reduction, silicidation or other undesired effects. Based on available tabulated thermodynamic data, only BeO, MgO and ZrO_2 are thermodynamically stable in contact with silicon at 1000 K. [1.17] For some more binary oxides, insufficient data is available to conclude that they are thermodynamically unstable in contact with silicon at 1000 K. This last group includes the high-κ oxides Al_2O_3, Y_2O_3, HfO_2 and Re_2O_3 (*Re* is a rare earth). Rare earth oxides of interest are Lu_2O_3, CeO_2, Pr_2O_3, Tb_2O_3, Dy_2O_3 and Gd_2O_3. Table 1.4 shows the periodic table of elements, with the location of elements which have thermodynamically stable binary oxides on silicon.

Table 1.5 shows the elements used in (the most common) high-κ binary, ternary and complex oxides. Preferred metals in metal oxides for high-κ dielectrics are Y, La, Hf and Zr. Disadvantage of for example Ti and Ta is its reactivity with silicon to form silicides and silicates. Disadvantage of e.g. Y_2O_3 is its high diffusivity of oxygen, which will react with the silicon substrate to form a silicon oxide interface layer. The dielectric should be permeable to hydrogen to allow passivation in surface state anneals, but not to oxygen.

Process integration of the new dielectric material requires the ability to pattern (etch) the material for contact holes. Changing the order of process

group	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
period																		
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	71 Lu	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	103 Lr	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Uub	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo
Lanthanoids			57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb		
Actinoids			89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No		

Table 1.4: elements with (probable) thermodynamically stable binary oxides on silicon at 1000 K, that are acceptable for integration with silicon. [1.17]

group	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
period																		
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	71 Lu	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	103 Lr	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Uub	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo
Lanthanoids			57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb		
Actinoids			89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No		

Table 1.5: elements of most high-κ binary oxides: Al_2O_3, TiO_2, Y_2O_3, ZrO_2, HfO_2, Ta_2O_5, La_2O_3 [1.15]; CeO_2 [1.18]; Pr_2O_3 [1.19]; Gd_2O_3 [1.20, 1.21]; Tm_2O_3, Nd_2O_3, Sm_2O_3, Eu_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 [1.22, 1.23].

group	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
period																		
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	71 Lu	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	103 Lr	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Uub	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo
Lanthanoids			57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb		
Actinoids			89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No		

Table 1.6: elements of some reported epitaxial high-κ oxides on Si(001): Al_2O_3 [1.24,1.25]; Y-stabilized ZrO_2 (YSZ), Y-stabilized HfO_2 (YSH) [1.26]; Y_2O_3 [1.27], CeO_2, Pr_2O_3, Gd_2O_3 [1.28].

steps or selective deposition of the gate stack are less trivial solutions. One important and undesired property of high-κ gate dielectrics is the (apparent intrinsic) reduction of inversion layer mobility. This issue has been reported to be due to fixed charge at the Al_2O_3/SiO_x interface, which induces Coulomb scattering. [1.29, 1.30] Other explanations have been found in Coulomb interaction of electrons in the channel with electrons in the depletion layer of the gate [1.31], dopant (boron) diffusion into the oxide [1.32] and remote phonon coupling to inversion layer charge. [1.33] A second issue is the so-called Fermi level pinning at the poly-Si/high-κ interface due to metal-silicon bonds [1.34], which effectively results in the polysilicon gate to be replaced by different metal gates for NMOS and PMOS devices.

Finally, epitaxial layers are of interest because of its control of defect chemistry, chemical stability, higher channel mobility and low interface trap density. Table 1.6 shows the elements of high-κ dielectric materials, which have been reported to be epitaxially deposited on Si(001). Materials that are suitable for epitaxial growth are “silicon derived” oxides and perovskites: materials with a small lattice mismatch with silicon.

1.3 Deposition techniques

Although thermal oxidation may still be used to fully oxidize deposited thin metal layers, replacement of SiO_2 by a high-κ dielectric will introduce new process techniques to the semiconductor technology. Deposition of gate dielectrics in the front-end of the process is a more critical step than deposition of metal interconnects in the back-end of the process. The requirements of uniformity and thickness control, step coverage and defect density will exceed that of traditional thermal oxidation.

Clearly, not all deposition techniques are suitable to deposit thin gate dielectric films. Some of the disqualifying factors are restrictions of the thermal budget, excess of energy of the deposited material and inherent contamination. Two deposition techniques will be briefly discussed in the following sections: pulsed laser deposition and atomic layer deposition. Chapters 2 and 3 include more detailed discussions and results obtained with these two techniques.

1.3.1 Pulsed laser deposition

The pulsed laser deposition (PLD) technique is a vapor deposition method, in which a laser is used to evaporate the source material. The pulsed laser beam

creates a dense vapor layer of target material on the target surface. The vapor absorbs most of the energy in the laser pulse and is transformed to an energetic plasma. The plasma will expand due to the pressure and temperature gradients, and a plume is formed of a characteristic shape. By placing a substrate inside or near the plume of evaporated material, condensation of source material can occur. The plasma is very reactive with O_2 in the chamber, thus the deposition ambient affects the deposited material.

The first use of laser energy to evaporate material and deposit thin films (in a vacuum system) was already reported in 1965. [1.35] Continued research resulted in numerous publications on successful deposition of oxides, semiconductors and superconductors. [1.36] Although the versatility of the PLD technique has been gratefully used in material science, semiconductor industry has not yet employed this technique in its production process.

Thin epitaxial layers can be deposited by PLD, but this depends on substrate quality and particle kinetics. Advantage of PLD is its ability to (locally) deposit exactly 1 unit cell, under the right process conditions, resulting in a smooth surface. Deposition of a metal oxide material is possible by using a metal target and an oxygen ambient. Single crystalline target materials result in a higher quality deposited layer, because of a lower impurity density in the target. To avoid craters in the target surface, the laser beam is scanned across the surface or the target is rotated. Typical specifications of commercially available excimer lasers are pulses of 20 ns, frequencies up to 100 Hz and a pulse energy up to 700 mJ. [1.37]

1.3.2 Atomic layer deposition

Growth by atomic layer deposition chemistry, using metal chlorides and water vapor, was first reported by Aleskovskii in 1965. [1.38] Since then, three different names have been used in literature for (more or less) the same deposition technique: atomic layer chemical vapor deposition (ALCVD™), atomic layer deposition (ALD) and atomic layer epitaxy (ALE). The latter is sometimes misused when the deposited material is not an epitaxial layer. The abbreviation for atomic layer chemical vapor deposition has been trademarked by ASM International. Therefore, atomic layer deposition has now become the preferred name for the deposition technique.

The ALD process of metal oxides is based on the sequential exposure to oxidizing and reducing precursor vapors. The precursor molecules, e.g. the reducing ones, saturate the surface by chemisorption. This process is limited

by the amount of suitable, available and accessible bonding sites. A second precursor is used as an oxidizing agent, removing ligands of the first precursor molecules on the surface and creating new bonding sites for the first precursor. Successful layer-by-layer growth is achieved by sequential repetition of both steps and avoiding gas phase reactions between both precursors. The deposition rate, or growth-per-cycle, is considered to be constant during the deposition of the layer (except for the initial coverage of the sublayer). The deposition is not sensitive to gas purge times, as long as they are long enough to saturate the surface.

1.4 Alternative solutions

Numerous techniques are available to deposit materials on a substrate. None of them can match the simplicity of thermal oxidation of silicon to form silicon oxide. Low pressure CVD, plasma enhanced CVD and sputtering techniques are widely used for other process steps in the semiconductor technology. Although a CVD process might exist for deposition of the high-κ material, the thickness and uniformity requirements of the gate oxide are generally not met. The formation of metal oxides by sputtering a thin metal layer and subsequent oxidation, has been published and shows promising results. However, the bombardment of the substrate by high energetic particles results in a mobility reduction by defects and subsurface implanted metal atoms.

The need of a new gate oxide for CMOS technology, is also a motivation for research on completely different solutions for logic circuitry. Prefixed by the scientific buzzword “nano”, several new techniques to operate digital information have been presented. Examples of futuristic transistors include optical switches, single electron transistors [1.39] and carbon nano-tubes. [1.40] However, it will take years (and years if at all) before multimillion transistor circuits can be manufactured with sufficient reliability. The current state of this research is still the development of full functionality of a single transistor.

A change in geometry of CMOS structures (e.g. vertical structures [1.41] or dual gate devices) might solve or suspend some of the barriers of downscaling, and is more easily utilized by the semiconductor industry. Although alternative structures are not directly a solution to the gate dielectric problem, the change in electric field might be an advantage for the implementation of high-κ dielectrics.

1.5 Conclusions

The development of semiconductor technology has reached several barriers in the downscaling trend of conventional CMOS transistors. A solution for the high leakage current of nanometer thick silicon oxide layers can be found in replacement by a high-κ dielectric material. Up to now, no combination of material and process has been found to match the electrical properties of thermally oxidized silicon and be suitable for full integration into the semiconductor technology. Although a long list of requirements and preferences is easily formed, the realization of an alternative process to create a suitable gate oxide appears to be very difficult.

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2 Pulsed laser deposition

A deposition technique is a process in which material is removed from a reservoir and applied to a sample. The energy, required for controlled transportation of the material, can be supplied in various ways from various sources. The result should be a layer of specified thickness, uniformity, composition, roughness, stability, ..., and any other preferred layer or material property. The intrinsic properties are usually only known for the bulk material and are difficult to replicate in deposited thin films. Deposition techniques are complicated processes with numerous interrelated parameters that all affect the final result.

2.1 Introduction

Pulsed laser deposition (PLD) has become an interesting technique for (high-κ) material research, due to its flexible use of multiple target materials and ability to deposit epitaxial layers. The use of an external laser as energy supply allows reduction of the reactor volume and avoids a possible source of contamination, e.g. sputter guns or filaments in evaporation systems.

A laser beam is focussed by lenses to a sufficiently high energy density to evaporate target material. The laser spot creates a dense vapor layer of target material in front of the target surface. [2.1] This vapor absorbs most of the energy of the laser pulse and is transformed to an energetic plasma of target material. The plasma will expand due to the pressure gradient and a plume is formed of a characteristic shape. A substrate can be placed near or inside the plume of excitated material to deposit a layer of the evaporated material. Figure 2.1 shows a schematic drawing of a PLD system.

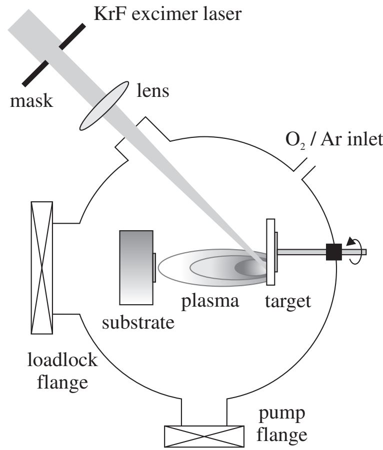


Figure 2.1: schematic drawing of the PLD system.

Different types of lasers can be used as energy source for PLD. In general, the laser is pulsed at frequencies up to 100 Hz with pulse lengths of 20 ns. The off-state of the laser allows deposited material to move to energetically favorable positions on the surface. Depending of substrate quality and particle kinetics, thin epitaxial layers can be deposited. Adjustment of all parameters eventually allows the deposition of exactly one unit cell of a crystalline material.

The plasma of excitated material is very reactive with an O_2 ambient in the reactor chamber. Metal oxides can be deposited from a metal oxide target, but also from a metallic target in an oxygen ambient. Complex materials can be deposited from composite targets or by sequential use of different targets. Single crystalline target materials result in a higher quality deposited layer, because of the lower amount of impurities in the target.

This chapter presents the results of experimental work on pulsed laser deposition of Al_2O_3 gate dielectrics. The goal of this work was to determine the suitability of pulsed laser deposition as deposition technique for high-κ gate dielectrics. Section 2.2 shows the results from finding suitable process conditions and the effects of (some of the) process parameters on the deposited layers. Several films have been deposited under the optimized conditions and have been characterized using different analysis techniques. The thickness, composition and surface morphology are discussed in section 2.3. The last sections of this chapter present results from electrical characterization of de-

vices with PLD Al_2O_3 gate dielectrics, followed by a discussion on the interface stability of the deposited layers and the suitability of PLD as a technique for gate dielectric deposition.

2.2 Deposition conditions

The feasibility of pulsed laser deposition of high-κ dielectrics was studied, using a single crystalline $(11\bar{2}0)$ α-Al_2O_3 (sapphire) target. A KrF excimer laser (Lambda Physik Compex, $\lambda = 248$ nm) was used to evaporate material from the target, at typical frequencies of 1 - 5 Hz and with a 20 ns pulse length. The uniformity of the energy density in the laser beam was improved by a 102 mm^2 diaphragm mask. The remaining pulse energy of about 130 mJ (measured directly after the lens) was focussed on the target to an energy density of 4.0 J/cm^2 and 2.9 mm^2 spot size. The 6.5 MW power of a laser pulse is (more than) sufficient to evaporate solid material from the single crystalline target. The process parameters for the first deposition attempts have been extracted from literature reports on PLD of crystalline (Ti_2O_3 doped) Al_2O_3 by a KrF excimer laser. [2.2–2.4] This material has also been deposited using lasers of different wavelengths. [2.5, 2.6]

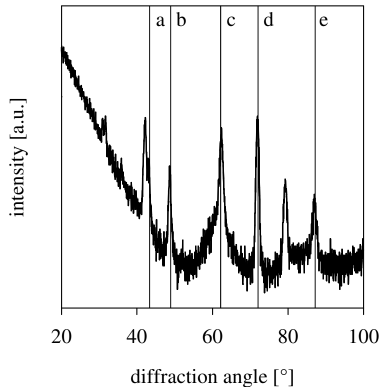


Figure 2.2: X-ray diffraction at diffraction angles 2θ, with identification of α-Al_2O_3 lattice planes: a. $(11\bar{2}3)$, b. $(02\bar{2}3)$, c. $(02\bar{2}6)$, d. $(03\bar{3}3)$, e. $(02\bar{2}4)$.

Figure 2.2 shows the X-ray diffraction scan (Philips XRD Expert system II, Cu K_α, $\lambda = 1.5405$ Å) of one of the first deposited layers of 1000 pulses. The first 50 pulses have been deposited at 10^{-6} mbar background pressure to

avoid substrate oxidation, followed by 950 pulses in 0.1 mbar O_2 ambient. The substrate was placed at the (visible) edge of the plasma plume, parallel to the target surface. This substrate to target distance was estimated to be about 42 mm. After deposition, the sample was cooled down from the deposition temperature (600 °C) in 4 mbar Ar ambient. The peaks in the XRD figure indicate the presence of multiple crystalline phases in the layer. Some peaks have been identified as possible responses to α-Al_2O_3 lattice planes. Other peaks should be attributed to some of the many other possible crystalline phases, e.g. γ-Al_2O_3. [2.7] The sample has been measured under a 5° tilt to avoid a large response to the silicon (004) plane at $2\theta = 69.13°$.

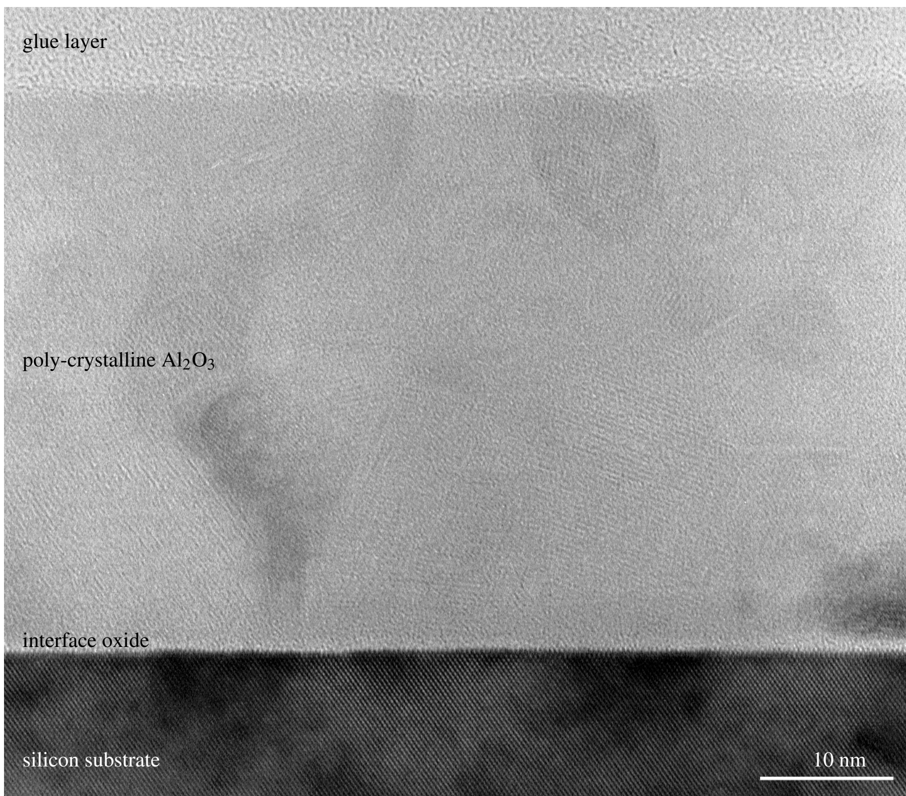


Figure 2.3: high-resolution (500k×) phase-contrast TEM image.

The poly-crystalline structure of the deposited film is clearly visible in the high resolution transmission electron microscopy (Philips CM30 Twin/STEM) image in figure 2.3. Although the first 50 pulses have been deposited at back-

ground pressure, an interfacial oxide layer has formed between the silicon substrate and the Al_2O_3 layer. The deposition rate was about 0.43 Å/pulse, as extracted from the thickness is in the TEM image. Figure 2.4 shows selective area diffraction patterns, as measured on the TEM sample. Bright spots appear around the center spot (direct transmission) on constructive interference of electrons on lattice planes. Figure 2.4b shows the additional spots due to crystalline Al_2O_3, compared to the pattern of the silicon substrate in figure 2.4a. The two images 2.4c and 2.4d show the diffraction patterns obtained from individual crystals. The difference in order of rotational symmetry is clearly visible.

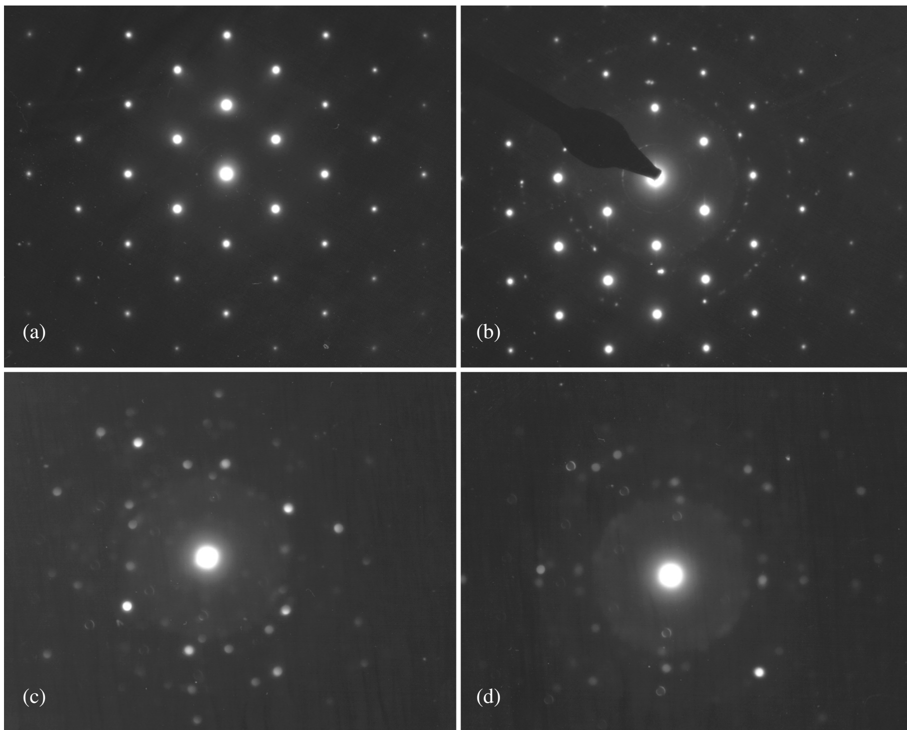


Figure 2.4: Selective area diffraction patterns of: (a) silicon substrate, (b) both silicon substrate and polycrystalline Al_2O_3. The <001> direction of the silicon substrate is upwards. Images (c) and (d) are nano-diffraction patterns (beam size 34 nm) of single Al_2O_3 crystals.

Poly-crystalline films are not desirable for gate oxide applications, since the crystal boundaries form conduction paths and result in higher leakage cur-

rents compared to amorphous layers. The deposited layer is poly-crystalline, although the 600 °C deposition temperature is below the reported [2.8] crystallization temperature of about 870 °C for amorphous Al_2O_3. This means the required additional energy is obtained from kinetic energy of the deposited material or from the energetic plasma plume. To avoid crystallization of the deposited layer and reduce interface formation, the deposition temperature has been decreased to room temperature for all experiments. In principle, the process window of pulsed laser deposition includes temperatures (far) below room temperature.

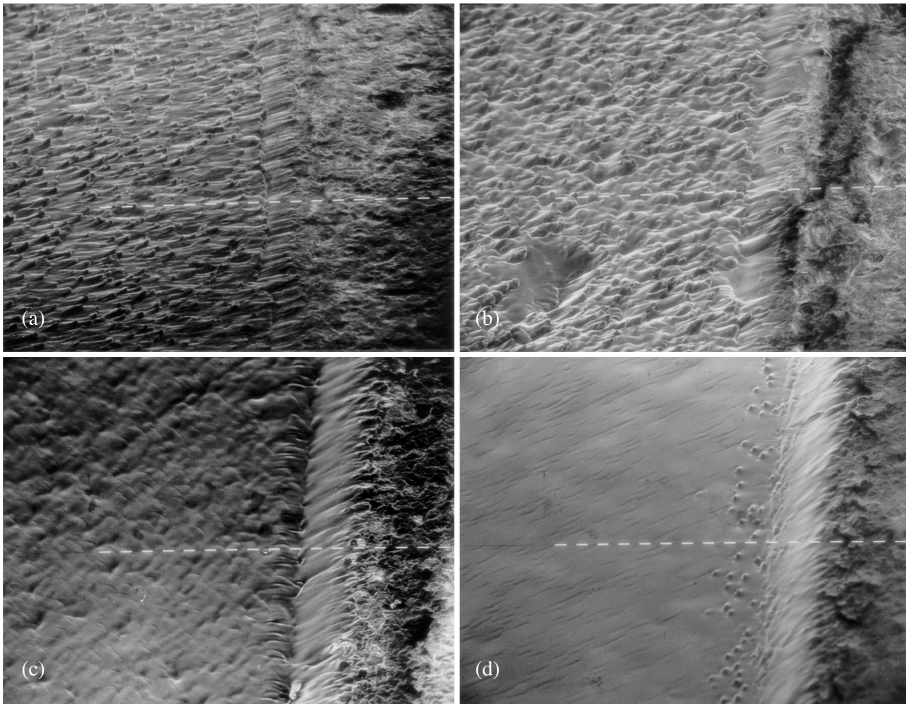


Figure 2.5: SEM images of the α-Al_2O_3 surface at 200× magnification, after 1000 pulses at a fixed position (left side of the image) and with energy densities: (a) 0.8 J/cm^2, (b) 1.0 J/cm^2, (c) 2.0 J/cm^2 and (d) 4.0 J/cm^2.

The ablated material arriving at the sample surface exchanges thermal and kinetic energy with the (heated) sample. The main energy source of deposited particles is the laser pulse and not the substrate heater. The laser pulse creates a dense vapor of target material in front of the target surface, but most of the laser energy is absorbed by the vapor layer. [2.1] This transforms the ablated

material into an energetic plasma. Although some of the kinetic energy is lost between the target and the substrate, excess energy of deposited particles allows rearrangement on the surface to energetically favorable positions. This can result in higher quality films (surface roughness), but can also lead to crystallization and other surface reactions. Adjustment of the energy of particles arriving at the sample surface is possible by the reactor pressure, the substrate - target geometry (distance, angle) and the energy of the laser pulse. The lower limit of the laser energy is determined by inspection of the target surface after ablation.

Figure 2.5 shows scanning electron microscopy (SEM) images of the target surface, after ablation (on the left side of the image) at different energy densities. The first image shows that material can already be evaporated with a low energy density of 0.8 J/cm^2. The laser fluence threshold for evaporation of target material has been reported to be about 0.5 J/cm^2. [2.9, 2.10] The morphology of the surface indicates the start of droplet formation from resolidified material. Although this effect is considered undesirable in a PLD process, the short depositions for thin layers (and polishing of the target surface) is not expected to result in deposition of droplets on the sample surface. Increasing the energy density of the laser pulse up to 4.0 J/cm^2 results in recrystallization of the target surface. The smooth surface of the last image is an indication of (too) high temperatures and is expected to affect continuous depositions due to the changed transparency of the surface.

2.3 Characterization of thin films

The surface of the target crystal has been lapped with a diamond pad, to clean the target and reduce the optical transparency of the surface layer. This should improve the start of the ablation process and not affect the actual deposition. During deposition on silicon substrates, the target is rotated to avoid craters in the target surface. To reduce undesirable reactions of high energy particles with the silicon substrate, a laser energy of 95 mJ (behind the lens) was focussed to about 0.8 J/cm^2 on the target in further experiments.

Silicon substrates have been cleaned by standard cleaning (HNO_3-based) and native oxide was removed by 1% HF prior to clamping on the substrate holder and loading in the chamber. The substrates have not been heated (or cooled) during deposition. The substrate to target distance has been changed from 42 mm to 50 mm for all experiments (except for the data in figure 2.8). Figure 2.6 shows that the layers deposited under the new conditions are amor-

phous, compared to the layers from initial deposition (figure 2.2).

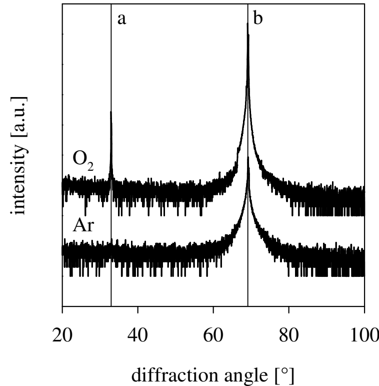


Figure 2.6: XRD scan at diffraction angles 2θ of samples (5000 pulses) deposited in Ar and O_2 ambient. The two peaks are due to diffraction on: a. Si(002) and b. Si(004).

2.3.1 Thickness

Figure 2.7 shows result of thickness measurements by ellipsometry (Plasmos SD 2002, 632.8 nm, 70°) at a fixed refractive index of 1.65. [2.11] The solid lines represent a linear least squares fit of the measured data. The linear fit is valid for deposition of the bulk of the layer, where the surface roughness is a fraction of the layer thickness and when a constant source of ablated material is assumed. Deposition in 0.1 mbar O_2 results in a thicker layer compared to deposition in 0.1 mbar Ar. The growth rate in O_2 is more than double the growth rate in Ar, indicating the reactivity of the plasma with an oxygen ambient. [2.12] This is also visually observed from the size and color of the plasma plume. Pulsed laser evaporation of a perfectly stoichiometric material results in a plasma of decomposed and reactive material. Therefore, the ambient of the deposition can change the composition of the deposited layer. The deviation of the measured thickness after 10 and 100 pulses is caused by the relatively thick interfacial oxide layer and inaccuracy of the ellipsometer for thicknesses below 10 nm. The dashed lines show the deviation of the linear fit when an offset is included.

The size of the plasma plume depends on the pressure in the reactor. Figure 2.8 shows the effect of substrate to target distance and reactor pressure, on

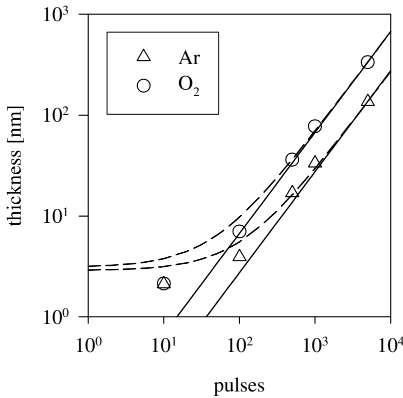


Figure 2.7: thickness of the deposited layers as measured by ellipsometry (n = 1.65). The solid lines represent linear least squares fits: $2.7{\cdot}10^{-2}$ nm/pulse in Ar ambient and $6.6{\cdot}10^{-2}$ nm/pulse in O_2 ambient. The dashed lines show the deviation of the linear fit when a positive offset is included.

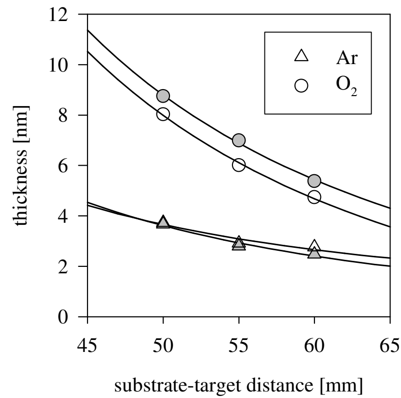


Figure 2.8: thickness of layers deposited at different substrate to target distances. The open and closed symbols represent depositions at 0.1 and 0.2 mbar, respectively.

the thickness of the deposited layer after 100 pulses. The lines represent least squares fits of the measured data, assuming the thickness to be proportional to the reciprocal squared distance, $t \propto d^{-2}$. Increasing the reactor pressure, results in a thicker layer of the sample deposited in O_2 ambient.

2.3.2 Composition

X-ray photoelectron spectroscopy (XPS) is a very suitable characterization technique to determine the composition and chemical bonding of deposited layers. Figure 2.9 shows two wide spectra measurements (PHI Quantum 2000, Al K_α, $h\nu$ = 1487 eV) of thick PLD layers (5000 pulses). The main peaks correspond to Al and O binding energies. The level of detected carbon contamination (at the surface) is typically caused by manual sample handing, sample transport and storage. The shape of the Al peaks indicates both layers are fully oxidized. Surprisingly, deposition in an O_2 ambient is not required for full oxidation of the aluminum atoms, but still results in an increase in deposition

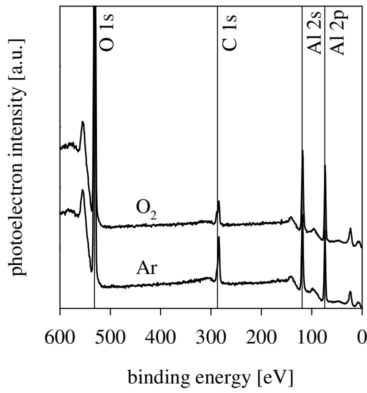


Figure 2.9: XPS wide spectra measurements of thick PLD Al_2O_3 layers, deposited in O_2 and Ar ambients. The offset of the spectra is only for clarification.

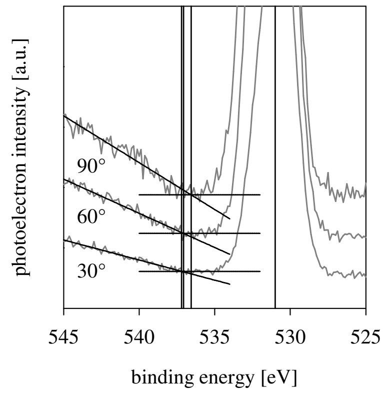


Figure 2.10: XPS measurement of the O 1s peak at three angles and extraction of the energy bandgap.

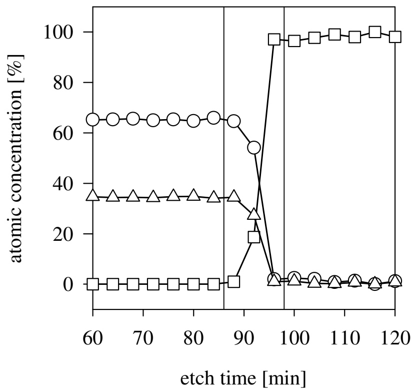


Figure 2.11: XPS depth profile of the sample deposited in Ar ambient. The sample was etched by 1 keV Ar^+ sputtering at about 2.5 nm/min.

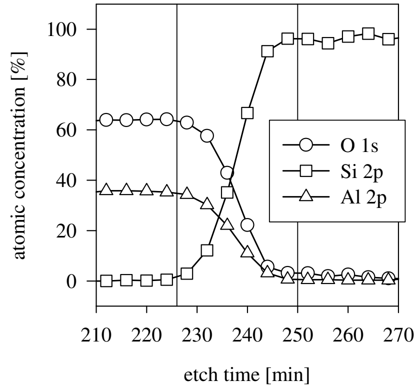


Figure 2.12: XPS depth profile of the sample deposited in O_2 ambient. The interfacial layer appears to be thicker compared to figure 2.11.

rate.

The energy bandgap of deposited materials can be extracted from the energy loss spectra of the O 1s peak. [2.13] Figure 2.10 shows parts of the measured O 1s peaks at 30°, 60° and 90°. The extracted energy bandgaps are 6.5, 6.2 and 5.2 eV, respectively. Although the extraction method can easily result in errors of ±0.2 eV, a large deviation is measured from the energy bandgap of 8.7 eV in figure 1.3.

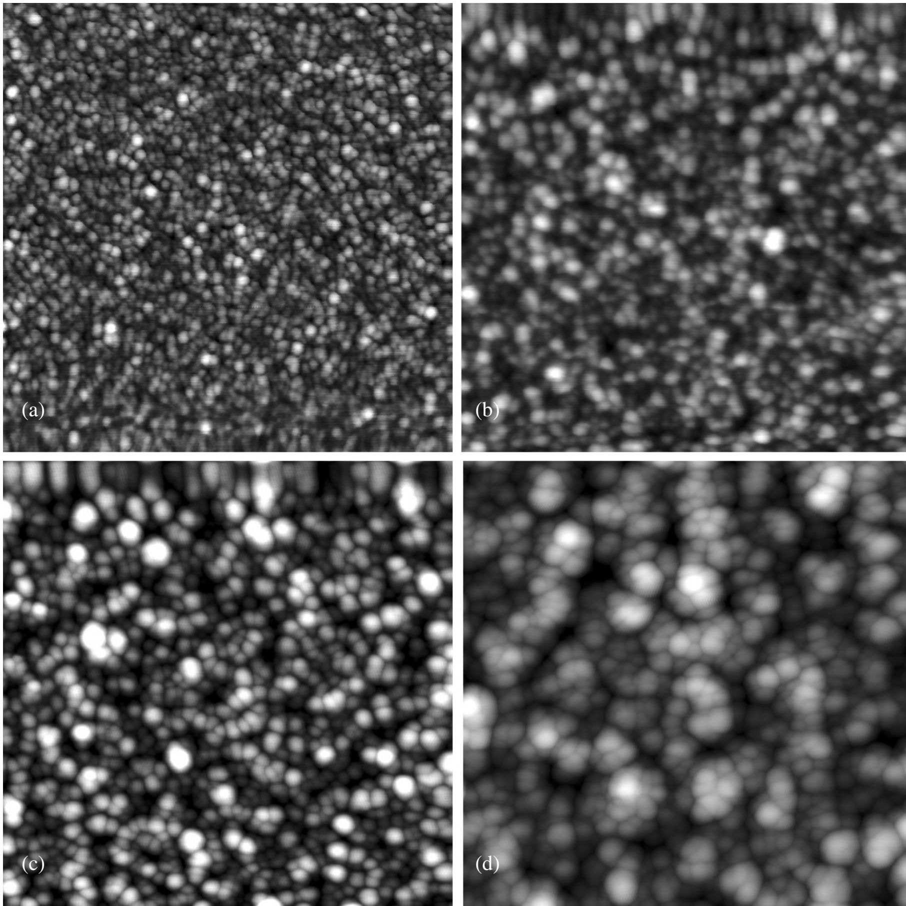


Figure 2.13: AFM images of the sample surface (1×1 μm) after: (a) 1000 pulses in Ar [5.7 nm], (b) 5000 pulses in Ar [10.6 nm], (c) 1000 pulses in O_2 [26.3 nm] and (d) 5000 pulses in O_2 [63.5 nm]. The Z-range is indicated between square brackets.

A depth profile of the deposited layer is derived from sequential peak mea-

surements and etching by 1 keV Ar^+ sputtering. Although the mean free path length of electrons and redeposition of sputtered material affect the measured profiles, interesting information can be extracted from the profiles in figures 2.11 and 2.12. The atomic concentrations of aluminum (65%) and oxygen (35%), corrected with their sensitivity factors, indicate the 2:3 ratio of stoichiometric aluminum oxide. The interfacial layer, between deposited layer and silicon substrate, appears to be thicker for the sample deposited in O_2 ambient. However, this result is affected by the difference in thickness and the roughness of the deposited layers.

2.3.3 Surface morphology

The surface of the samples has been studied using tapping-mode atomic force microscopy (Digital Instruments Dimension 3100 SPM). Figure 2.13 shows the AFM scans of samples after 1000 and 5000 laser pulses in Ar or O_2 ambient. The RMS surface roughness (R_q) of the scanned area is 0.69 nm, 1.48 nm, 3.44 nm and 8.44 nm, respectively. The surface roughness, normalized to the thickness, is decreasing with the number of pulses (see figure 2.14). This trend and the structure visible in the AFM scans are indications of island growth mode of the deposited layer. Deposition in O_2 ambient results in a higher surface roughness than deposition in Ar ambient.

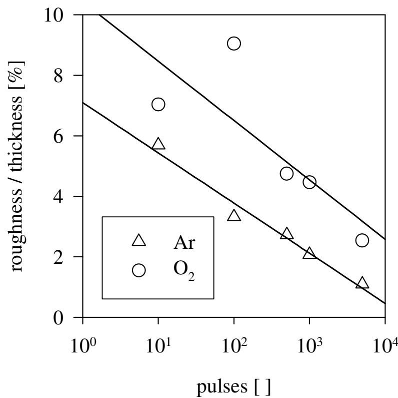


Figure 2.14: decrease in relative surface roughness with the number of pulses.

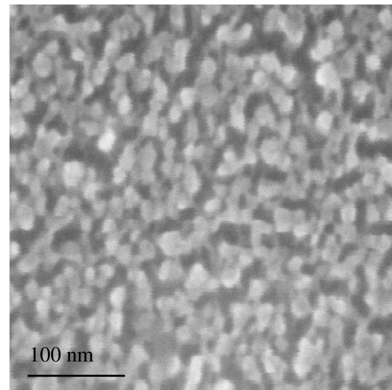


Figure 2.15: SEM image (168k×) of the surface after 500 pulses in O_2.

The scanning electron microscopy image (LEO Gemini 1550 FEG-SEM) in figure 2.15 confirms the surface morphology measured by AFM. An increase in dielectric thickness results in the buildup of more charge on the surface and is visible as a brighter spot on the SEM image.

2.4 Characterization of devices

The electrical characteristics of the PLD films have been measured using prefabricated samples with LOCOS and source/drain implants. The 100 mm wafers have been diced to 15×15 mm^2 samples, to fit the sample holder of the PLD system. After deposition of the Al_2O_3 gate dielectric, an aluminum metal gate was deposited and interconnect to source and drain was made. This process recipe was further developed for characterization of ALD high-κ dielectrics (chapter 6). The final version can be found in appendix C.

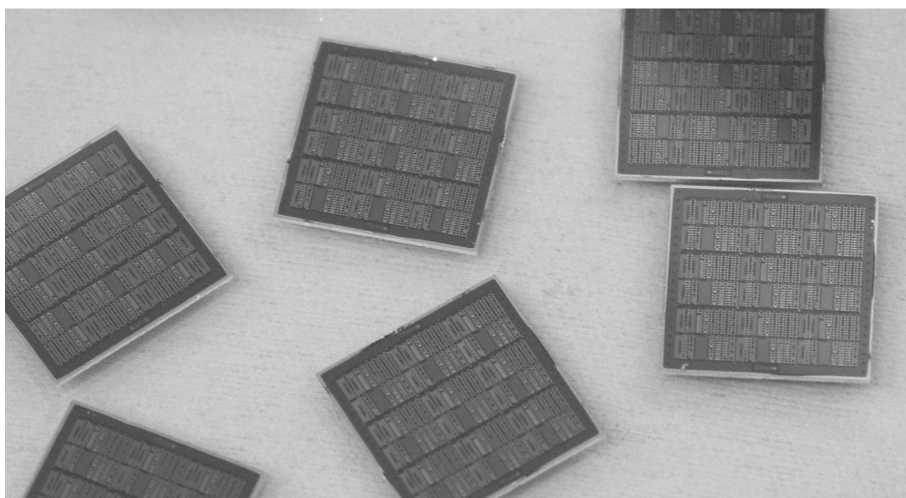


Figure 2.16: photograph of 15×15 mm^2 samples with PLD test structures.

The PLD Al_2O_3 layers in all samples with test structures have been deposited using a laser energy of 95 mJ (0.8 J/cm^2) and in 0.1 mbar O_2 or Ar ambient at room temperature. The substrate-target distance was about 50 mm for all depositions. The thickness of the PLD Al_2O_3 layers was estimated from the ellipsometry measurements in figure 2.7.

Leakage current measurements (Agilent 4156C semiconductor parameter analyzer) on 110×110 μm capacitor stacks, showed severe trapping and

de-trapping of charge during the voltage sweep. Although the current levels are low, as to be expected from these thick dielectric layers, the defect induced leakage current results in a dielectric breakdown at relatively low electric fields.

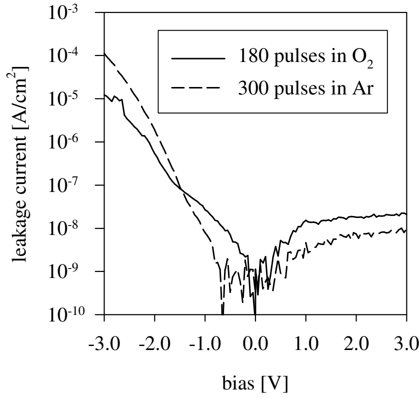


Figure 2.17: current-voltage characteristics.

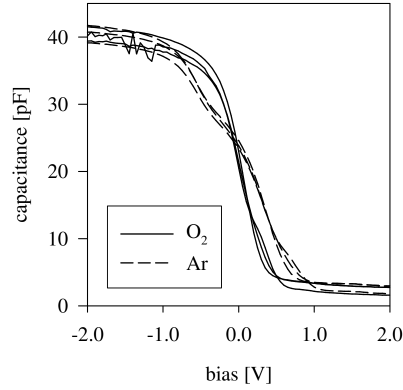


Figure 2.18: capacitance-voltage characteristics at 10 kHz, 100 kHz and 1 MHz.

High frequency capacitance-voltage measurements at 10 kHz, 100 kHz and 1 MHz (Hewlett-Packard 4284A LCR meter) show a consistent accumulation capacitance value of about 40 pF. The capacitance equivalent oxide thickness (see page 16) is about 10.4 nm. This thickness does not correspond well to the expected physical thickness (11.9 nm in O_2 and 8.1 nm in Ar), as based on the deposition rates determined in figure 2.7. The deviation in thickness is caused by a combination of factors: interfacial oxide thickness, parasitic capacitance (probe pads), voids in the layer and the effective thickness due to surface roughness.

The inversion layer mobility can be extracted from small-signal channel conductance measurements [2.14]

$$g_{\mathrm{ds}} = \left.\frac{\delta I_{\mathrm{ds}}}{\delta V_{\mathrm{ds}}}\right|_{V_{\mathrm{GS}}=\mathrm{const}} = \beta \cdot (V_{\mathrm{GS}} - V_{\mathrm{T}}) = \frac{\mu_{\mathrm{eff}} \cdot C_{\mathrm{ox}} \cdot W_{\mathrm{eff}}}{L_{\mathrm{eff}}} (V_{\mathrm{GS}} - V_{\mathrm{T}})\,. \tag{2.1}$$

The channel conductance g_{ds} was measured using a zero-bias high-frequency signal (10 mV, 1 MHz) from the LCR meter. A constant gate voltage V_{GS}

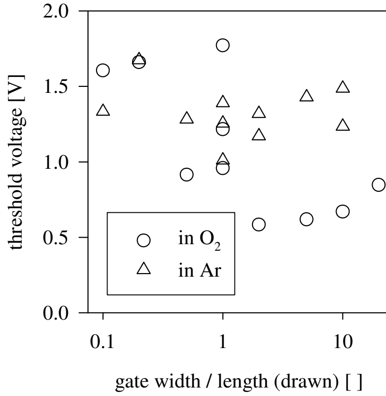


Figure 2.19: threshold voltage as extracted from g_{ds} measurements of samples deposited in O_2 (180 pulses) and Ar (300 pulses).

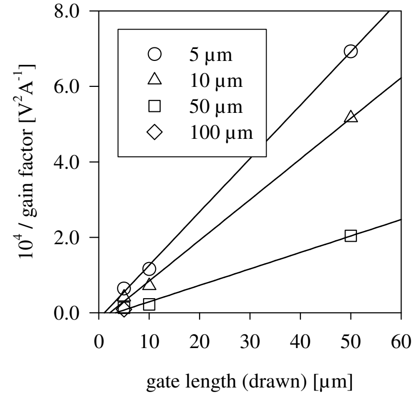


Figure 2.20: reciprocal gain factor β_0 of the O_2 sample, as function of drawn gate length for different gate widths.

was supplied by the 4156C semiconductor parameter analyzer. The threshold voltage (see figure 2.19) and the gain factor β (figure 2.20) are extracted from the measured g_{ds}-V_{GS} conductance characteristics. The low-field (zero-field) mobility μ_0 is calculated from the gain factors, using the gate oxide capacitance found in figure 2.18, and

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \vartheta \cdot (V_{GS} - V_T)}. \tag{2.2}$$

with gate bias mobility lowering factor ϑ.

The linear fits in figure 2.20 give inconsistent values, ranging from 426 $cm^2V^{-1}s^{-1}$ for a gate width of 5 µm to 138 $cm^2V^{-1}s^{-1}$ for a 50 µm wide gate. Single linear least squares fitting through the gain factors of all measured MOSFETs (as function of the gate ratio *L*/*W*), result in low-field mobility μ_0 values of 395 $cm^2V^{-1}s^{-1}$ and 525 $cm^2V^{-1}s^{-1}$ for the O_2 and Ar samples, respectively. A typical reference value (of interface layer electron mobility under SiO_2) close to 1000 $cm^2V^{-1}s^{-1}$ can be obtained from the universal curves. [2.15, 2.16]

2.5 Interface stability

Instability of the silicon/high-κ interface easily results in channel mobility degradation. The typical energy of laser ablated atoms is about 40 eV, which is relatively large compared to the 5 eV energy of sputtered atoms and 0.2 eV (300 K) of evaporated material. [2.17] The strength of atomic bonds is also in the order of only a few electronvolts. One possible cause of channel mobility reduction is the silicidation reaction, in which a metal atom from the oxide layer exchanges position with a silicon atom at the interface. In the silicon/Al_2O_3 system, the exchange of an aluminum and a silicon atom results in additional substrate doping with an acceptor ion. Subsequent diffusion could have severe effects on the electrical characteristics of the device.

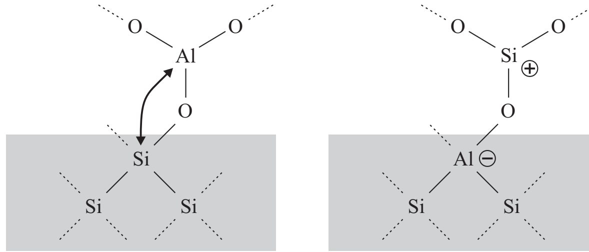


Figure 2.21: exchange of Al and Si atom positions.

bond	energy [kJ/mol]	energy [eV]
Al-Al	133 ± 6	1.38 ± 0.06
Al-O	511 ± 3	5.30 ± 0.03
Al-Si	229.3 ± 30.1	2.38 ± 0.31
Si-O	799.6 ± 13.4	8.29 ± 0.14
Si-Si	325 ± 7	3.37 ± 0.07
Ce-O	795 ± 8	8.24 ± 0.08
Hf-O	801.7 ± 13.4	8.31 ± 0.14
La-O	799 ± 4	8.28 ± 0.04
Ta-O	799.1 ± 12.6	8.28 ± 0.13
Ti-O	672.4 ± 9.2	6.97 ± 0.10
Y-O	719.6 ± 11.3	7.46 ± 0.12
Zr-O	776.1 ± 13.4	8.04 ± 0.14

Table 2.1: bond strength. [2.18]

According to thermodynamics, a reaction (at constant temperature and

pressure) is likely to occur for a negative change in Gibbs energy

$$\Delta G = \Delta H - T \cdot \Delta S < 0. \tag{2.3}$$

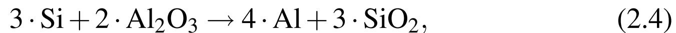
The change of entropy ΔS is positive, since the degree of disorder increases on Al diffusion into the silicon. Thus, the diffusion is likely to occur using chemical reactions with negative change in enthalpy ΔH. This change of enthalpy can be estimated from the sum of bond energies of broken and formed bonds. The bonds that are broken (see figure 2.21) are 3 Al-O bonds to release the aluminum atom, x Si-Si bonds and $(4-x)$ Si-O bonds, where x is 1 - 3. The bonds that are formed are 3 Si-O bonds, x Al-Si bonds and $(4-x)$ Al-O bonds.

With the values in table 2.1, the change of enthalpy is calculated (table 2.2) to be -3.0, -1.0 and +1.0 eV for exchange of an aluminum atom and a silicon atom with oxidation state x of 1, 2 and 3, respectively. The exchange between fully oxidized aluminum and silicon atoms, results in an enthalpy change of +3.0 eV. Based on the change of enthalpy, the exchange reactions of an aluminum atom with a silicon atom bonded to up to 2 oxygen atoms at the interface, is likely to occur.

Si state	bonds broken			bonds formed			ΔH
x	Al-O	Si-Si	Si-O	Si-O	Al-Si	Al-O	[eV]
0	3	4	0	3	4	0	-5.01
1	3	3	1	3	3	1	-3.01
2	3	2	2	3	2	2	-1.01
3	3	1	3	3	1	3	0.99
4	3	0	4	3	0	4	2.99

Table 2.2: change of enthalpy ΔH in the exchange reaction of a fully oxidized aluminum atom with a silicon atom at the interface.

Figure 2.22 shows the phase diagram of the Al-Si-O ternary system, with positions of reported aluminum silicates. [2.19, 2.20] All silicates are located on the line connecting SiO_2 and Al_2O_3. In table 1.4, Al_2O_3 was included as probable thermodynamically stable material, due to the absence of known aluminum silicides. In combination with the reported change in Gibbs free energy ΔG of +2.75 eV (at 1000 K) for the reaction



$$3 \cdot \mathrm{Si} + 2 \cdot \mathrm{Al_2O_3} \rightarrow 4 \cdot \mathrm{Al} + 3 \cdot \mathrm{SiO_2}, \tag{2.4}$$

Al_2O_3 is concluded to be stable on silicon. [2.19] Based on the metal-oxide bond strength (table 2.1), most of the other high-k dielectrics are more stable. However, excess energy during deposition is still expected to result in intermixing at the interface.

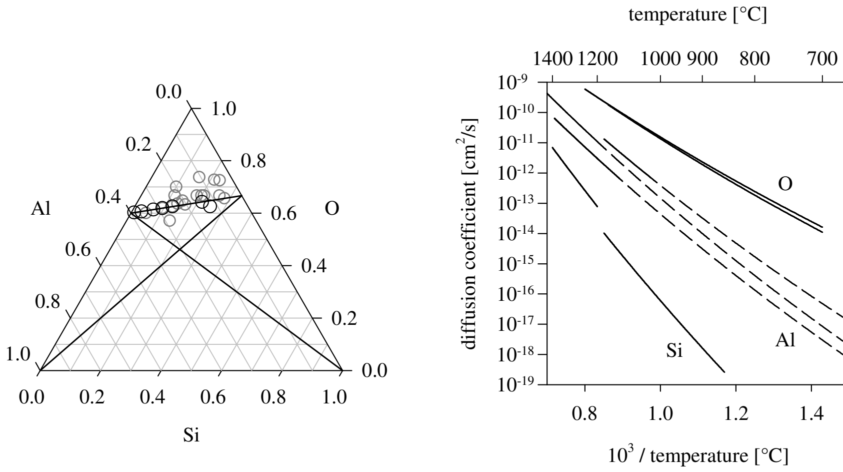


Figure 2.22: phase diagram of the Al-Si-O system with position of reported aluminum silicates (black [2.19] and grey [2.20]).

Figure 2.23: diffusion constants of Si, O and Al in silicon. [2.21] The center Al line is based on D_0 = 8.00 cm^2/s and E_A = 3.47 eV. [2.22]

The severity of aluminum intermixing with the substrate is quantified by the diffusion constant, the maximum solid solubility and the source concentration. The amount of aluminum atoms is limited to (part of) the first monolayer on the substrate, or the first pulse in the PLD process. Although limited information is known on the low temperature diffusion of aluminum in silicon, extrapolation of the data in figure 2.23 results in a diffusion constant D of about 10^{-22} cm^2/s at 500 °C. For a 1 hour deposition at 500 °C, $\sqrt{Dt}$ is in the order of several picometers, much less than a monolayer. Although the temperature contribution to aluminum diffusion is negligible, the kinetic energy of deposited particles is still sufficient to enhance diffusion.

The maximum solid solubility is about $5{\cdot}10^{18}$ cm^{-3} [2.23] at 500 °C (and equilibrium), which is about 10^{-4} of the density of silicon atoms in the substrate. This ratio indicates that there will be about 10^{11} cm^{-2} aluminum atoms at the interface, which results in a flatband voltage shift of only

$$\Delta V_{\mathrm{FB}} = -\frac{Q}{C_{\mathrm{ox}}} \approx 9\,\mathrm{mV}, \tag{2.5}$$

for an equivalent oxide thickness of 2 nm. However, the electron mobility is already reduced by ionized impurity scattering at lower concentrations. [2.24]

2.6 Conclusions

The pulsed laser deposition technique was successfully used to deposit Al_2O_3 gate dielectrics from a single crystalline sapphire target. Results from initial experiments at elevated temperature and with high-energy laser pulses, showed poly-crystalline Al_2O_3 layers and interfacial oxide. Adjustment to deposition at room temperature and with optimized laser energy, resulted in stoichiometric and fully oxidized amorphous layers, even for deposition in argon. Analysis of the surface morphology by AFM and SEM revealed an increase of surface roughness during deposition by growth of surface particles. This effect is amplified by deposition in an oxygen ambient, which results in thicker layers compared to deposition in argon under similar conditions. Electrical characterization showed disappointing results, initiating discussions on the suitability of PLD for gate oxide deposition.

The main disadvantage (second to the scalability issues) of the PLD technique is the high kinetic energy of deposited particles. The energy of ablated material is directly related to the laser energy required to evaporate material on the target. Undesired surface reactions of deposited material should be avoided by reduction of its kinetic energy. This may be achieved by substrate cooling, increasing the substrate-target distance or increasing the ambient pressure. Also, the laser wavelength and the type of target affect the kinetic energy of ablated material: e.g. a pure aluminum target in an oxygen ambient may result in better Al_2O_3 layers.

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Part II

Experimental

3 Atomic layer deposition

The design of a new system is the result of an engineer's imagination, shaped by a long list of known requirements and limitations of costs and construction. Several design revisions eventually result in the construction of an experimental version. During the fabrication and testing of the experimental system, the list of requirements is extended with (some) previously unknown items. In a research project with only one possibility to construct an experimental system, the challenge is to look beyond the newly found design requirements and focus on the research issues.

3.1 Introduction

The approach to contribute to solving the gate dielectric problems, is to study the growth of metal-oxide layers in an improved ultra-clean atomic layer epitaxy (UC-ALE) technology. The improvements should allow preparation of the surface and controlled initial growth on an atomic level to study the material related problems. In-situ characterization tools during growth consist of reflection high-energy electron diffraction (RHEED) at the surface and mass spectrometry of gases in the reactor. Additionally, an ultra high vacuum connection is available to transport samples to an attached system with scanning probes (STM/AFM) and X-ray photoelectron spectroscopy (XPS) analysis capabilities. This summary of the project proposal briefly describes the goal, motivation and direction of the project. The work in this dissertation is focused on the atomic layer deposition system and in-situ growth characterization.

As already mentioned in section 1.3.2, the ALD process of metal oxides is based on the sequential exposure to oxidizing (oxygen supplying) and reducing precursor vapors. In principle, the ALD technique is suitable for deposition of single element and compound materials. For all materials, at least one precursor should saturate the surface by chemisorption. This process is limited by the amount of suitable, available and accessible bonding sites on the surface. The chemisorbed layer of precursor molecules should be stable (no desorption or decomposition) and allow surface preparation in a sequential process step for repetition of the ALD cycle. Figure 3.1 shows a step-by-step graphical presentation of the ALD process.

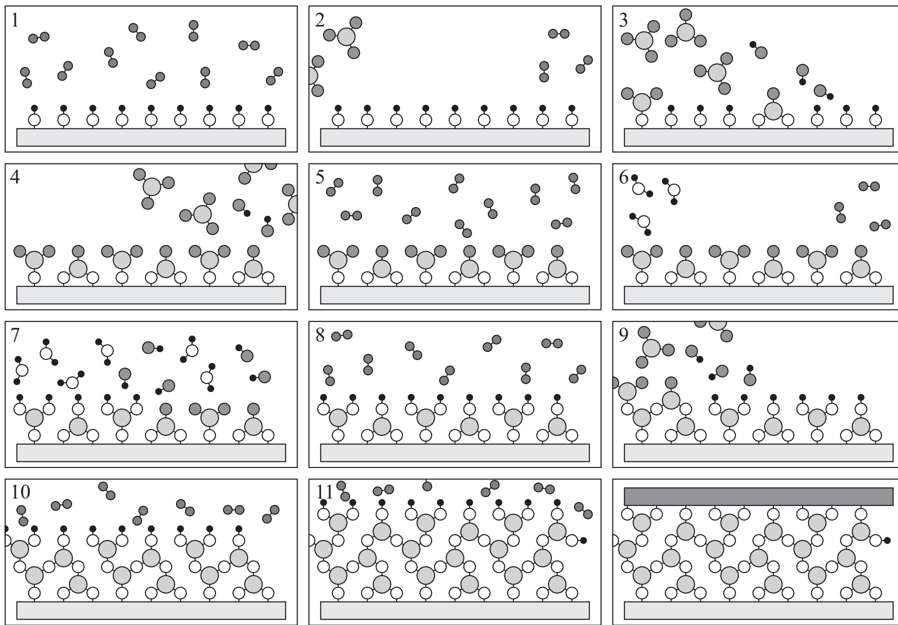

Figure 3.1: step-by-step presentation of the ALD process, with: 1. stable hydroxylated Si surface in inert (N_2) ambient, 2. exposure to first precursor, 3. chemisorption of precursor creates volatile byproduct, 4. surface saturation, 5. purge of remaining precursor and byproduct, 6. exposure to second precursor, 7. removal of ligands and creation of new bonding sites, 8. purge of remaining precursor and volatile byproduct (ligands of first precursor), 9. exposure to first precursor in the second ALD cycle, 10. surface after two deposited layers, 11. surface after three deposited layers, 12. gate stack of three deposited layers.

The second precursor is used to remove ligands (e.g. methyl groups of

$Al(CH_3)_3$) of the first precursor molecules on the surface and to create new bonding sites for the first precursor. This can be an oxygen supplying agent (H_2O, H_2O_2, O_2, O_3) for deposition of metal oxides, a precursor for deposition of other compounds (sulfides, nitrides, ...) or a strictly ligand removing precursor for deposition of single element materials. [3.1, 3.2] The latter can also be used in the rare case when all material for a compound is supplied by a single precursor. Layer-by-layer growth can be achieved by successful surface preparation for chemisorption of the first precursor in the next ALD cycle. Deposition rate, or growth-per-cycle, is considered to be constant during the steady state (bulk) deposition of the layer.

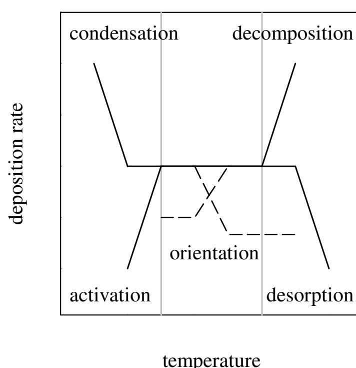

Figure 3.2: process window of atomic layer deposition chemistry.

The deposition temperature of an ALD process should provide the activation energy for chemical bonding of precursor molecules to the surface sites. Especially for evaporated solid precursors, the deposition temperature should be high enough to avoid condensation of the precursor on the sample surface and parts of the reactor (including gas supply lines). The upper limit of deposition temperature is determined by desorption and decomposition of the chemisorbed precursor molecules. The remaining process window (figure 3.2) can be over 100 °C wide, sometimes split by temperature ranges with different growth rates due to ligand orientation. Large molecule precursors might be able to align their ligands at elevated temperatures to a higher density on the surface (i.e. reconstruction). The temperature windows of the first and second precursor chemistry can be (very) different. Some ALD processes require an additional form of energy (plasma, light, ...) or catalyst for one of the reactions, because the temperature windows do not overlap.

The two precursors should be applied sequentially for saturation limited layer-by-layer growth. To avoid gas phase reactions between the two precursors or with reaction by-products, intermediate purge steps with an inert gas are necessary. The purge time should be sufficient to remove all reactive gas phase molecules. Chemisorbed precursor molecules should be stable enough to stay bonded to the surface. The efficiency of the purge step can be improved by a combined, sequential or intermediate pump down of the reactor.

3.2 Design of the ALD system

The first drawings of the system showed a three reactor system with loadlock and transport mechanism. After processing the sample in the ALD reactor, vacuum connections would allow the sample to be transported to the other two reactors for either XPS or AFM/STM analysis. Gradually, this design was changed to benefit more projects by sharing the control units and infrastructure. Advantages of a larger system are an increase in system usage, additional capabilities and a reduction in overall costs.

The so-called "cluster system" now consists of a large loadlock connected to three ALD-capable single wafer reactors: 1. low temperature plasma enhanced deposition of dielectrics, 2. deposition of metallic layers (TiN) and 3. deposition of high-κ dielectrics (Al_2O_3). Two experimental LPCVD batch reactors are separated from this system, but share the control units and gas systems. The ALD reactor (3), which will be described in further detail below, has an additional valve to exchange samples with an analysis system for XPS and AFM/STM measurements. The analysis system has its own control units, but is connected to allow transport of samples without vacuum break.

The deposition systems are controlled by an industrial computer, running a dedicated Labview application. This application is able to control/monitor all pneumatic gas valves, the throttle valves, the gate valves and robotic arm for sample transport, the turbo pump controllers, the temperature controllers and read the (pressure) sensors. Pneumatic gas valves are used in a common gas system to provide the five reactors with a choice of available semiconductor technology gases. Additionally, pneumatic valves are used to pulse the reactive gases for the ALD process. A programmable sequence controller is used for the ALD process, to avoid time lag by overload of the processor in the control system.

Figure 3.3: photograph of the loadlock (front) with three ALD systems, from left to right: 1. low temperature plasma enhanced deposition of dielectrics, 2. deposition of TiN layers and 3. deposition of Al_2O_3 dielectrics with in-situ RHEED system.

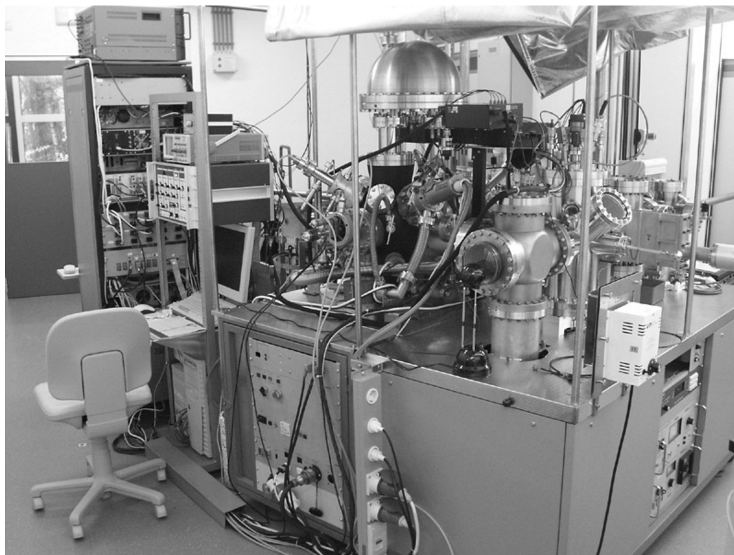

Figure 3.4: photograph of the XPS and scanning probe analysis systems.

3.2.1 ALD process chamber

The cylindrically shaped reactor chamber (figure 3.5) has two DN160CF (155 mm inner diameter, metal sealed) flanges for sample transport, at opposite sides on the reactor wall. One of the flanges is used to accept a sample from the loadlock through a gate valve. The second flange is used to transport the sample to the analysis system after deposition. Perpendicular to the valves forming a transport line, are two more flanges for the RHEED analysis setup. This part will be discussed in chapter 4. A DN100CF flange is used for feed through of four gas lines for reactive gases and one nitrogen gas line for purging and venting of the reactor. Finally, the wall of the reactor chamber has four DN40CF flanges for the connection of pressure sensors and electrical feed through for the thermocouple and heaters.

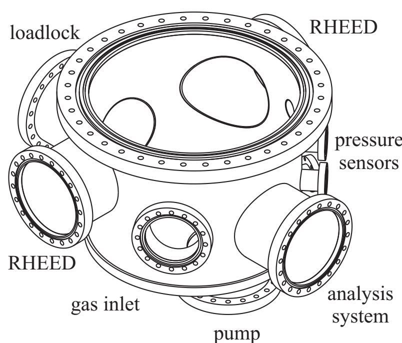

Figure 3.5: schematic drawing of the reactor chamber with description of flange connections.

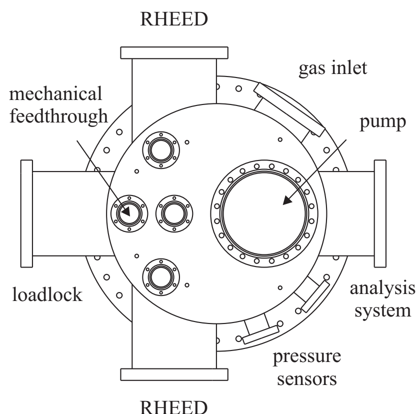

Figure 3.6: schematic drawing of the bottom side of the reactor chamber.

The bottom of the reactor chamber (figure 3.6) has a DN160CF flange for connection of a throttle valve and turbo molecular drag pump (Pfeiffer Vacuum TMH1000C, magnetic bearing, corrosion resistant, 1000 l/s). The turbo pump is connected to a dry backing pump (Alcatel ACP28G, corrosion resistant, 27 m^3/h). Additionally, four small flanges are used for mechanical feed through to the inner parts of the reactor. The top of reactor chamber is closed by a large lid, with either a metal or O-ring seal. The latter type of sealing is especially useful when the reactor has to be opened and closed repeatedly, but also results in a higher background pressure.

A smaller process chamber is mounted inside the relatively large reactor chamber. This inner reactor chamber is mainly used to reduce the volume that has to be filled with reactive gas. This reduction is required to reduce the gas consumption and increase the deposition rate of the ALD process by minimization of the saturation and purge times. The inner reactor basically consists of three elements (see figure 3.8): a gas block, a cover and a sample holder.

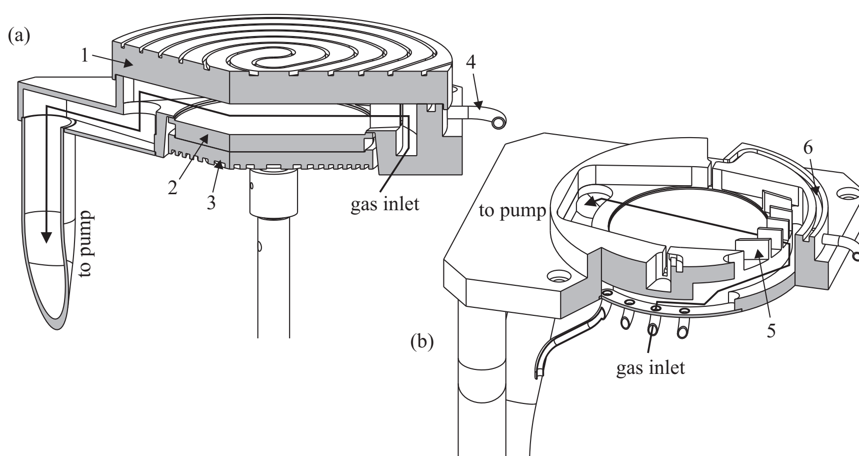

Figure 3.7: schematic drawing of inner reactor (a) and gas block (b) with: 1. heated cover of process chamber, 2. wafer tray, 3. heated chuck, 4. N_2 inlet for purge of RHEED openings, 5. gas flow channels, 6. N_2 purge flow channel.

The gas block (figure 3.7) is a metal plate with an approximately 100 mm hole, to form the side walls of the inner reactor. This hole is closed at the top-side by the thermocoax (80 V, 1 kW, 1000 °C max.) heated cover. A wafer (or smaller sample) is transported on a wafer tray, which after loading is pressed against the bottom side of the gas block. This closes the small volume of the inner reactor, with the wafer as large part of the total inner surface. The lever, which is used to close the inner reactor with the wafer tray, the pedestal, is also thermocoax heated to reduce temperature gradients.

The main task of the gas block is feeding the reactive gases to the sample. To that purpose, the four gas lines of the feed through in the outer reactor chamber are connected to a common gas channel in the gas block. This channel originates from the design idea to create a nitrogen lock near the sample, to avoid gas phase reactions between reactive gases. The gas channel is now mainly used to direct the gas flow uniformly over the sample, regardless of

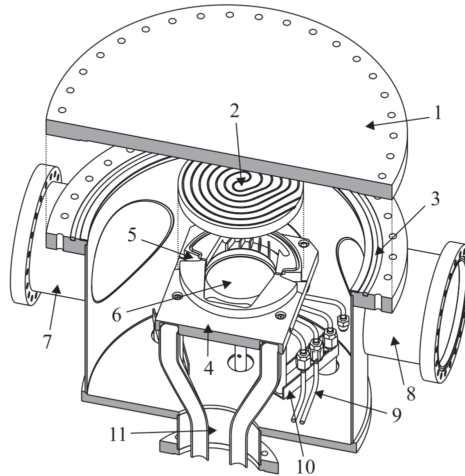

Figure 3.8: schematic drawing of the ALD reactor, with: 1. cover of reactor, 2. heated cover of process chamber, 3. metal or O-ring seal, 4. gas block, 5. slit for electron beam RHEED system, 6. wafer tray, 7. flange for fluorescent screen, 8. flange for electron source, 9. gas lines, 10. tilt capability of process chamber, 11. flange for throttle valve and pump.

which of the four feed lines is used. Because of the experimental stage of the gas block, it can easily be removed and replaced.

The reactive gas which is fed to the inner reactor is pumped at the opposite side. Two tubes are attached to the gas block and extend into the DN160CF flange to just above the throttle valve (see figure 3.8). Since the throttle valve opens on the side just below these tubes, at (high) process pressure the pump will effectively pump more of the reactive gases from the inner reactor than from the outer reactor. This effect is enhanced by a fine grating around the two tubes, closing the remaining part of the pump flange, and is used as a restriction between the pump and the outer reactor chamber.

To study the growth behaviour during processing, the reflection high-energy electron diffraction (RHEED) analysis technique was implemented in the ALD reactor. The use of a RHEED system during ALD has large implications on the design of the gas block and the outer reactor chamber. These will be discussed in chapter 4. Figure 3.9 shows the two arms to transport samples to the loadlock (left) or to the analysis systems (right).

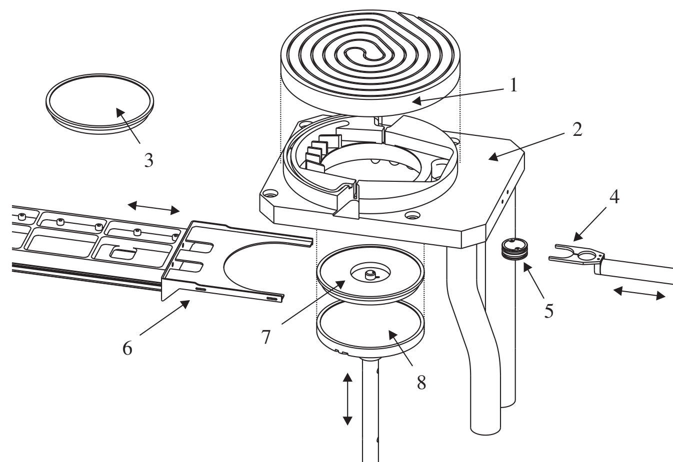

Figure 3.9: schematic drawing of the sample transport, with: 1. heated cover of process chamber, 2. gas distribution block, 3. wafer tray for 100 mm wafers, 4. fork for sample transport to analysis system, 5. sample holder for cm^2 samples (XPS and SPM), 6. robot arm with fork for transport of wafer tray from the loadlock, 7. adapter (wafer tray) for sample holder, 8. heated chuck for wafer tray.

3.2.2 Precursor handling

Numerous solutions are available for sequential exposure to different precursors, with or without intermediate purging to avoid gas phase reactions. The main differences are the use of static or moving substrates (move between two precursor streams) and the use of mechanical shutters or inert gas barriers. [3.3] In experimental lateral flow reactors, the obvious solution to switch reactive gases is a combination of shutters (gas valves) and inert purge gas. The additional gas valves reduce precursor consumption, compared to inert gas valving with a continuous precursor flow. The construction of the precursor valving also depends on the state (solid, liquid, gas) of the precursors.

A basic combination of two valves, to direct the precursor flow to the reactor or bypass the flow directly to the pump, is suitable for CVD reactors but not for the ALD process. The source valve is usually located outside (but close to) the reactor. The gas line between the valve and the reactor is a dead volume when the valve is closed and still a diffusion source of the reactant. This would result in gas phase reactions between the remaining gas flow and the sequential pulse of the second precursor.

Dead volumes with remaining precursor can be avoided by flushing with

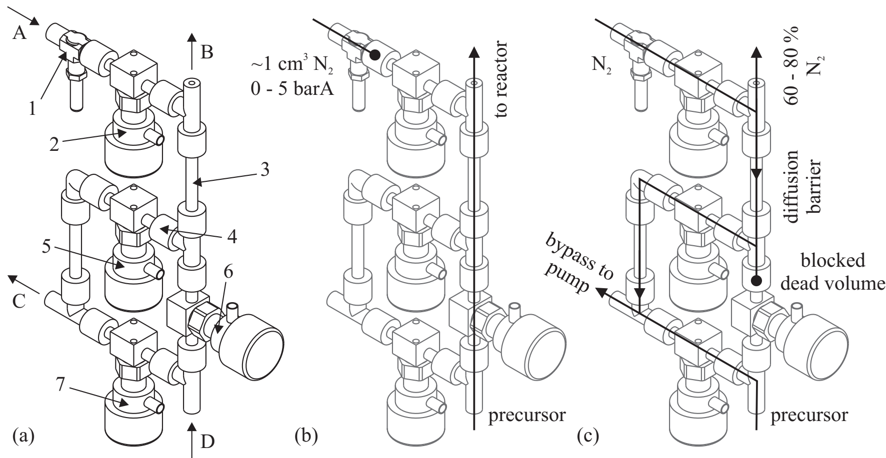

Figure 3.10: schematic drawing of the precursor valves with gas line connections (a): A. N_2 purge gas inlet, B. outlet to deposition chamber, C. bypass outlet to pump and D. inlet of precursor. The other components are: 1. needle valve to restrict flow of purge gas (continuous), 2. valve for purge gas (barrier source), 3. diffusion barrier, 4. orifice gasket to divide purge flow between bypass and reactor, 5. valve for purge gas (barrier drain), 6. source valve for precursor, 7. bypass valve for precursor. Figures (b) and (c) show the working principle during the precursor pulse and the purge step, respectively.

an inert gas. However, depending on the volume and the precursor, this can be a time consuming step. A better method is to create a flow of inert gas in the opposite direction of the diffusing reactive gas. The blocking nitrogen flow is bypassed to the pump at the end of this diffusion barrier. Flow restrictions allow adjustment of the blocking flow through the diffusion barrier and the purging flow through the reactor.

The required length of the diffusion barrier depends on the diffusion coefficient of the precursor (see table 3.1 and figure 3.11), the gas line diameter and the barrier flow. The calculation is based on the difference in speed of the diffusion front and the barrier flow, and can be found in appendix A. A diffusion barrier for H_2O vapor in a ¼ inch gas line with N_2 gas, requires a length of 3.2 cm for ppb-level suppression of H_2O diffusion to the reactor.

Finally, valves should be added to the design to be able to close the bypass line (barrier flow), isolate the precursor containers (for exchange) and flush the precursor lines. The diffusion barrier valve combination can not be used to pulse an MFC-controlled gas. The blocking flow in the diffusion barrier and

ambient	D_0 [10^{-2} cm^2/s]
air	25.18
N_2	22.60
H_2	85.37
He	80.49
CH_4	24.30

Table 3.1: diffusion coefficients of H_2O vapor in different ambients at 293.2 K and normal (atmospheric) pressure. [3.4]

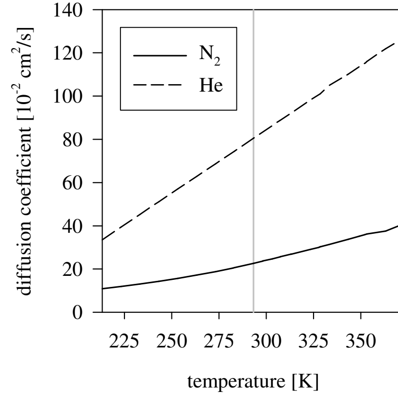

Figure 3.11: temperature dependence of the diffusion coefficients of H_2O vapor in nitrogen and helium ambients.

the restriction in the bypass will have a large impact on the stability of the gas flow. Figure 3.10 shows the construction with the four pneumatic valves for each gas line: *barrier source* valve (2), *barrier drain* valve (5), *reactor* valve (6) and *bypass* valve (7).

During the precursor pulse, only the reactor (precursor) valve is opened. The small volume between the needle valve (1) and the barrier source valve (2) is filled with about 0 bar N_2 (gauge pressure). At the end of the precursor pulse, the reactor valve is closed and the barrier valves (2 and 5) are opened. The relatively high pressure N_2 will expand quickly (explode) to purge the gas lines towards the reactor and through the diffusion barrier (3). During the purge time, the needle valve restricts the continuous flow of purge gas. The bypass valve (7) is only opened for MFC-controlled precursors when the reactor valve is closed, i.e. during purge steps and pulses of other precursors.

The two liquid precursors for Al_2O_3 ALD, trimethylaluminum $Al(CH_3)_3$ (Shipley, OptoGrade TMA) and water (demineralized), have sufficient vapor pressure to be used without carrier gas. A carrier gas can be used to transport the precursor vapor to the reactor and may be required to transport sufficient precursor in the allowed exposure time. Figures 3.12 and 3.13 show the gas line schematics of the ALD reactor and gas supply system. The carrier gas reduces the partial vapor pressure of precursor in the container, thereby increas-

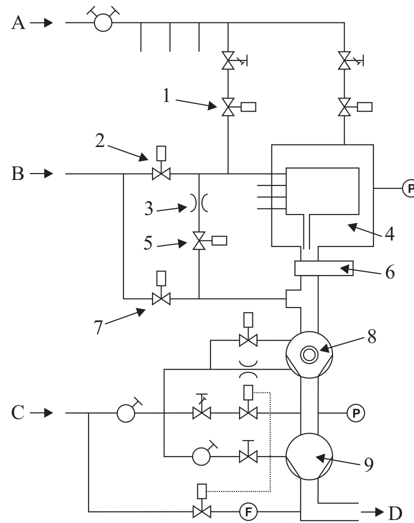

Figure 3.12: schematic drawing of the ALD reactor, with: A. N_2 purge gas inlet, B. precursor inlet, C. N_2 purge inlet to pumps and D. outlet to exhaust system. The other components are: 1. barrier source valve, 2. precursor source valve, 3. orifice, 4. reactor with deposition chamber, 5. barrier drain valve, 6. throttle valve, 7. bypass valve, 8. turbo molecular pump, 9. backing pump.

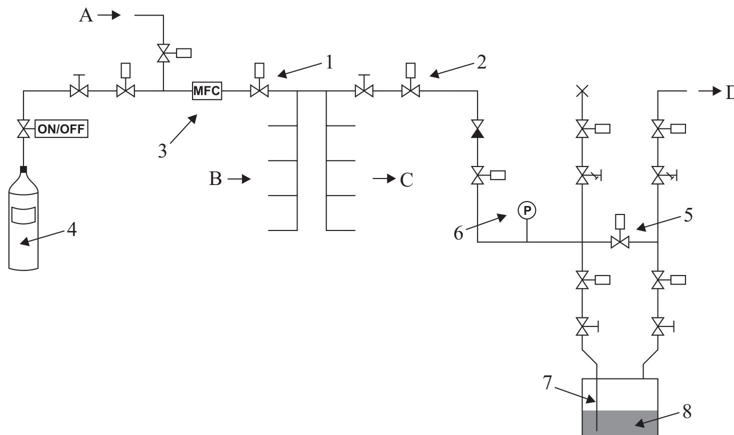

Figure 3.13: schematic drawing of the precursor supply, with: A. N_2 purge gas inlet, B. manifold for 5 gases, C. manifold to 5 reactors and D. outlet to reactor. The other components are: 1. gas selection valve, 2. reactor selection valve, 3. mass flow controller, 4. gas bottle, 5. liquid precursor bypass, 6. liquid precursor vapor pressure sensor, 7. dip tube, 8. liquid precursor.

ing the evaporation rate of the precursor. The vapor pressure is calculated from its molar heat of vaporization ΔH_{vap} and its boiling point T_{bp} (at atmospheric pressure, p_{bp} = 1013.25 mbar), by

$$\ln\left(\frac{p}{p_{\text{bp}}}\right) = \frac{\Delta H_{\text{vap}}}{R} \cdot \left(\frac{1}{T} - \frac{1}{T_{\text{bp}}}\right). \tag{3.1}$$

Figure 3.14 shows the temperature dependence of the vapor pressure and the measured pressures at the used temperature setpoints.

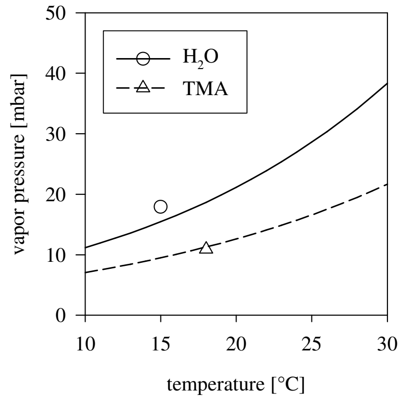

Figure 3.14: vapor pressure curves of liquid precursors TMA and H_2O, according to equation 3.1. The symbols indicate the measured pressures at the used temperature setpoints.

3.3 Characterization of the reactor

After construction of the experimental system described in the previous section, the behavior of the system was characterized. This section presents the results from pump curve measurements, temperature characterization, determination of the deposition rate and finally the uniformity of the deposited layers.

3.3.1 Gas flow and pump capacity

Figure 3.15 shows the relation between reactor pressure and nitrogen flow (through the bypass). The pressure was measured using full range gauges (cold

cathode $5{\cdot}10^{-9}$ - 10^{-2} mbar, Pirani $5{\cdot}10^{-3}$ - 10^{3} mbar) for high vacuum (HV) measurement and a Baratron gauge (capacitive diaphragm, 10^{-2} - 10^{3} mbar) for process pressure (PR) and backing pressure (BK) measurement.

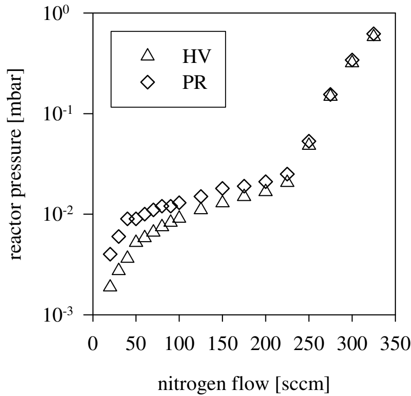

Figure 3.15: reactor pressure measured as function of nitrogen flow, using the high vacuum (HV) and process (PR) pressure sensors.

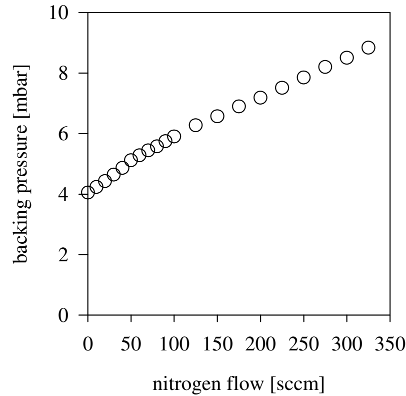

Figure 3.16: backing pressure (BK) measured as function of nitrogen flow.

Figure 3.16 shows the measured foreline pressure (between the backing pump and the turbo molecular pump) at different nitrogen flows. The maximum fore vacuum of the turbo molecular pump is 11 mbar according to specifications. The pressure-flow characteristics are used to determine the performance of the system under normal operation. The pump curves have been recorded with a Pfeiffer Vacuum MVP160 backing pump (8.3 m^3/h), which was later replaced by a Adixen ACP28G pump (27 m^3/h). This allowed the N_2 dilution flow of the reactive gases to be increased, without compromising the characteristics in figure 3.16.

The precursor flow was determined by measurement of the foreline pressure and subsequent conversion to an equivalent N_2 flow, using the data in figure 3.16. The amount of precursor flow is determined by the pressure in the reactor, the vapor pressure of the precursor, the evaporation rate and finally, the conductivity of the gas line between the precursor bottle and the pump. The latter can be changed by a needle valve, located near the precursor bottle (see figure 3.13). Figure 3.17 shows the bottle pressure as function of the needle valve position. The decay is the result of precursor flow to the pump,

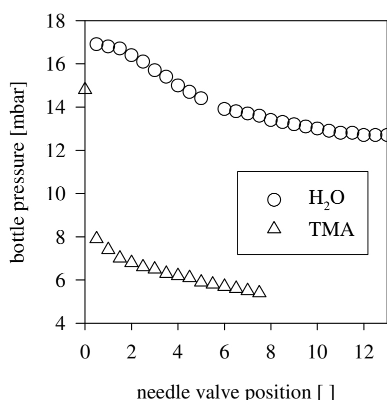

Figure 3.17: precursor bottle pressure as function of needle valve position.

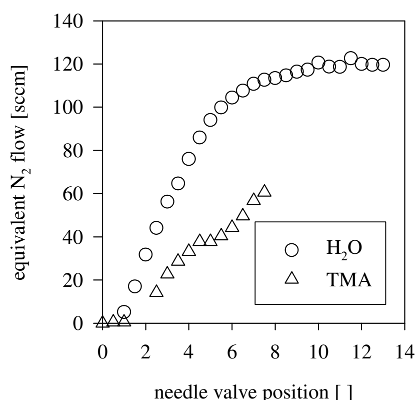

Figure 3.18: equivalent nitrogen flow as function of needle valve position.

at a higher rate than the evaporation rate. The measurement is also affected by the location of the pressure gauge (between the bottle and the pump) and is therefore only a measurement of the local pressure. However, it does indicate a flow of precursor from bottle to reactor. The amount of precursor (in equivalent N_2 flow) is displayed in figure 3.18 and shows the H_2O flow to be about twice the flow of TMA. This difference in flow (at the same needle valve position) relates to the ratio of vapor pressures.

Based on the ideal gas theory, a precursor pulse of 10 sccm for 2 seconds contains about $8.2 \cdot 10^{18}$ molecules. This is roughly 160 times the number of silicon atoms at the surface of a 100 mm wafer. Without a good estimate of the efficiencies of the ALD chemistry and the reactor design, apparent excessive use of precursor might still result in underdosing on the wafer. However, the measured flow and pressure characteristics show that the reactor is capable of a wide experimental window and should be capable to obtain suitable ALD conditions.

3.3.2 Deposition temperature

The deposition rate of several atomic layer deposition processes has been reported to be constant in a large temperature range. However, the deposition temperature still affects the layer density, formation of interface layers and the incorporation of contamination (from ligands). Accurate temperature calibra-

tion of ALD systems is required to validate the comparison of experimental results.

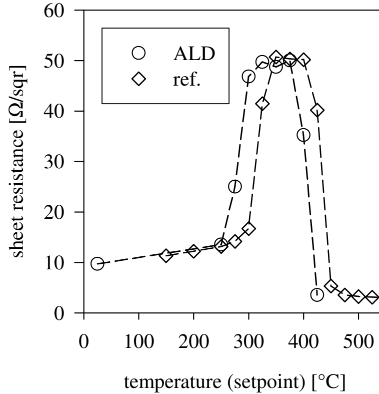

Figure 3.19: sheet resistivity characteristics of Co/Si stacks as function of the temperature setpoint of the ALD reactor and a calibrated vacuum system.

Figure 3.19 shows the result of temperature calibration measurements, using the change in sheet resistivity with temperature during cobalt-silicide formation. [3.5] This method can be used to determine the maximum temperature of samples that have been heated in a reactor. Several p-Si(001) wafers have been prepared by sputtering a stack of about 25 nm Co and 2 nm Si. Annealing this stack results in diffusion of Co in Si [3.6] and the formation of several cobalt and cobalt-silicide (CoSi, Co_2Si, $CoSi_2$) phases. [3.7] At temperatures up to 400 °C the sheet resistivity increases due to interdiffusion of Co in Si. The characteristic temperature dependence is probably related to solubility limits of Co in the thin silicon layer. At about 410 °C, the CoSi phase is formed [3.8] and a large reduction of sheet resistivity is observed. The $CoSi_2$ phase is formed at temperatures above 590 °C. [3.9]

The samples have been heated up in the ALD reactor to the temperature setpoint, for 20 minutes in 10 mbar N_2 ambient. After unloading and cooling down, the sheet resistivity was measured by a four-point probe setup. The reference data was obtained by in-situ measurements in a temperature calibrated vacuum system. The shift of the measured characteristic with respect to the reference curve, indicated a temperature deviation of about +40 °C. However, this is the maximum temperature of the sample and can be the result of a temperature overshoot.

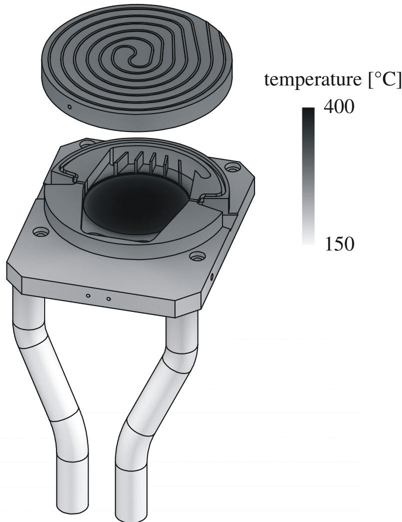

Figure 3.20: simulation result of finite element thermal analysis.

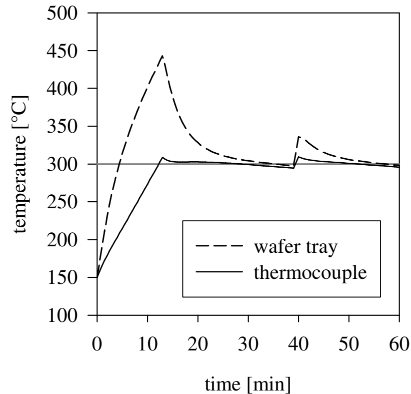

Figure 3.21: temperature of the wafer-tray and thermocouple (inside heated cover) during heating from 150 to 300 °C.

Figure 3.20 shows the result of a simplified thermal analysis, using finite element modeling software (CosmosWorks). Energy loss by gas flow through the reactor (forced convection), surface-to-surface radiation (wafer tray to cover and vice verse) and radiation to the outside environment have all not been taken into account. The modeled system consists of the gas block with (closed) heated cover and the heated pedestal with the wafer tray. Both heating elements have been set to generate 500 W each. The higher density of the bottom heating element and the lower mass of pedestal and wafertray, result in a higher temperature of the sample location (wafer tray), compared to the thermocouple location (heated cover).

The result of heating the reactor from 150 to 300 °C (thermostat ± 5 °C) is a large temperature overshoot of the wafer tray. Figure 3.21 also shows a temperature overshoot of the wafer tray of about 40 °C, when the reactor is already at its temperature setpoint. The loss of thermal energy has been simulated as a 1 W/(m^2K) arbitrary loss of the outside surface of the process chamber.

All results indicate that the actual temperature of the sample can be higher

than expected from the thermocouple measurement. A revision of the reactor design should change the difference in density of the two heaters, or change the power supply to allow individual control of each heater. Relocation of the thermocouple measurement point will not solve the temperature gradient in the reactor. The high temperature overshoot of the bottom heater can be avoided by changing the standby temperature to the deposition temperature (and loading the sample at the deposition temperature) or limiting the power of both heaters. The first option is expected to reduce the lifetime of the fluorescent RHEED screen (see chapter 4), but the latter option increases the heat up time to unacceptable values.

3.3.3 Uniformity

Successful layer-by-layer deposition in an ALD process with sufficient exposure and purge times, and full saturation of the surface, should in principle result in extremely uniform layers. Non-uniformity of the deposited layer can be attributed to one (or more) steps in the ALD cycle. Insufficient purge steps result in vapor phase reactions between precursors and an increase in deposition rate. Due to the limited amount of precursor available for vapor phase reactions, the increase in deposition rate might be localized and not be as distinct as expected. Incomplete saturation of one of the two precursors is easily related to the amount supplied (time or concentration) and usually clearly visible as a decay in thickness in the direction of the precursor flow.

However, not all uniformity problems are caused by (time) critical process recipes. Characterization of the experimental ALD reactor includes the determination of uniformity issues which are intrinsic to the design of the reactor. Basically, these issues are limited to temperature and gas flow. A large deviation of (local) temperature can result in decomposition of the precursor, condensation, desorption or insufficient activation energy (see figure 3.2). Gas flow related issues in a lateral flow reactor can cause local deposition to be determined by diffusion of precursor during both exposure and purge steps.

Figure 3.22 shows the thickness and within wafer uniformity (3-sigma) of several depositions of 100 ALD cycles, using the recipes in table 3.2, as determined by ellipsometry measurements (Plasmos SD 2002, 632.8 nm, 70°). The deposition pressure is controlled by the throttle valve between the reactor and the turbo pump, using the pressure gauge in the reactor. A higher pressure setpoint has several consequences for the deposition: the precursor flow is lower (depends on vapor pressure - reactor pressure difference), the residence time

	TMA / N_2	H_2O / N_2	
1	1.0	1.0	
2	1.0	1.0	*
3	1.0	2.5	
4	1.0	2.5	*
5	2.5	1.0	
6	2.5	1.0	*
*	5.0	5.0	

Table 3.2: pulse times of the experiments in figure 3.22. The asterisk (*) denotes experiments with prolonged pulse times (5.0 s) in the first 10 of 100 cycles.

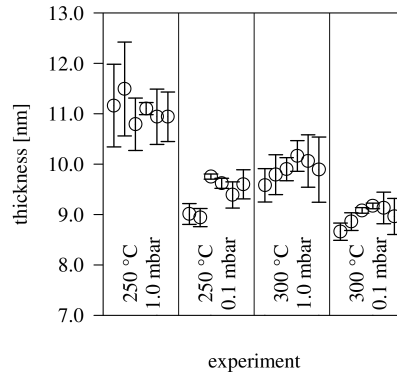

Figure 3.22: mean thickness and within wafer uniformity (3-sigma) of experiments (table 3.2) at different temperature and pressure.

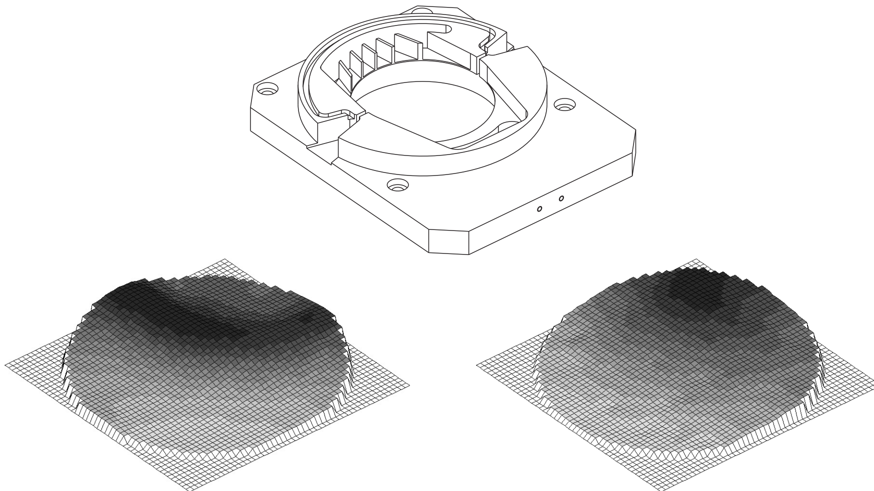

Figure 3.23: uniformity of the deposited Al_2O_3 layer (250 °C, 1.0 mbar, 1.0 s pulses); the grayscale range is 10.70 - 12.57 nm.

Figure 3.24: uniformity after deposition at 300 °C and 0.1 mbar; the grayscale range is 8.83 - 9.28 nm.

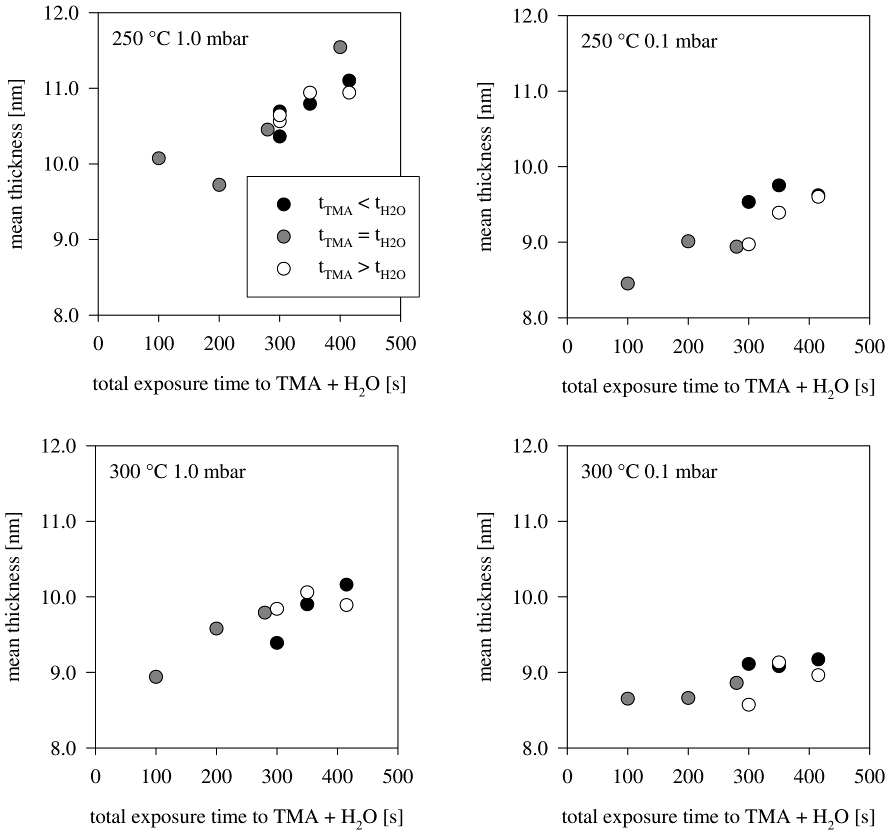

Figure 3.25: thickness as function of the total exposure time to TMA and H_2O, at different temperature and pressure. The color of the symbols indicates if the exposure time to TMA was shorter, longer or equal to the exposure time to H_2O.

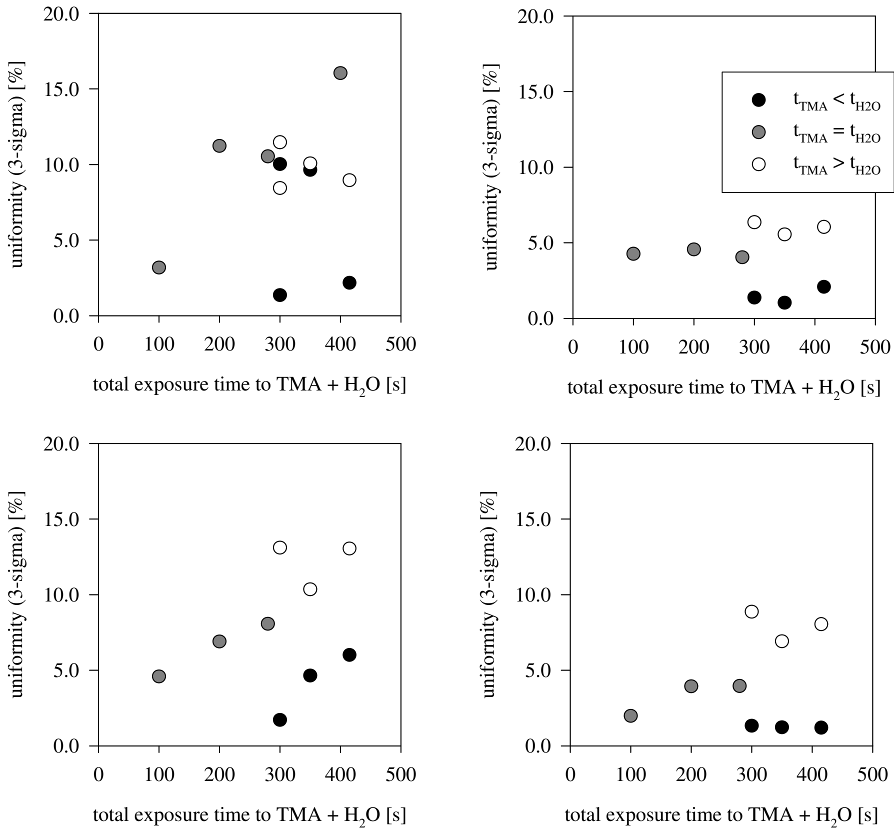

Figure 3.26: uniformity (3-sigma) as function of the total exposure time to TMA and H_2O, at different temperature and pressure. The color of the symbols indicates if the exposure time to TMA was shorter, longer or equal to the exposure time to H_2O.

of precursor molecules in the reactor is longer and the purge is less efficient. Especially the latter effect clearly results in a decrease in uniformity. The advantage of the ALD chemistry is that the deposited thickness is more or less constant under a wide range of process conditions.

The figures 3.23 and 3.24 show the uniformity pattern of the deposited layer for two deposition conditions: 250 °C 1.0 mbar and 300 °C 0.1 mbar. The gas block is displayed to indicate the relation between uniformity pattern and the design of the deposition chamber.

In figures 3.25 and 3.26 the mean thickness and 3-sigma within wafer uniformity are plotted as function of the total exposure time to reactive gas (TMA + H_2O) in a deposition of 100 cycles. The four graphs differ in pressure and temperature, similar to the graph in figure 3.22. Clearly, the preferred deposition condition is at low reactor pressure (0.1 mbar) and high temperature (300 °C).

Under this condition, the thickness depends only on the number of cycles and not on the precursor dose. The within wafer uniformity of the layers is clearly improved by increasing the H_2O pulse. A more likely explanation for this is the increased purge time, which is equal to the preceding pulse time.

	10 ×		90 ×		total
	TMA	H_2O	TMA	H_2O	exposure
1	0.5	0.5	0.5	0.5	100
2	1.0	1.0	1.0	1.0	200
3	5.0	5.0	1.0	1.0	280
4	0.5	2.5	0.5	2.5	300
5	2.5	0.5	2.5	0.5	300
6	1.0	2.0	1.0	2.0	300
7	2.0	1.0	2.0	1.0	300
8	1.0	2.5	1.0	2.5	350
9	2.5	1.0	2.5	1.0	350
10	2.0	2.0	2.0	2.0	400
11	5.0	5.0	1.0	2.5	415
12	5.0	5.0	2.5	1.0	415

Table 3.3: composition of total exposure time (in seconds) to reactive precursors (TMA and H_2O) in figures 3.25 and 3.26. In some experiments, the first 10 of the 100 cycles has prolonged exposure times.

3.4 Characterization of thin films

The growth rate has been obtained from layer thicknesses, as determined using angle resolved XPS measurements (Kratos XSAM 800, Mg K_α). X-ray photoelectron spectroscopy uses an incident low-energy X-ray beam, which (on absorption by the sample) results in the ejection of electrons via the photoelectric effect. The energy of the emitted electrons is characteristic of the type of atom (and its bonding state). The sampling depth of the XPS technique can be reduced by changing the angle between sample and analyzer. Comparing the intensities of peaks at the same kinetic energy at different angles allows the extraction of the layer thickness. Photoelectrons generated in sub-surface layers only emerge when their effective range (l_e) is larger than the length of the escape path.

The signal intensity from atoms at depth x varies as:

$$I = I_0 \cdot \exp\left(-\frac{x}{l_\mathrm{e} \cdot \cos(\phi)}\right), \tag{3.2}$$

where ϕ is the angle between the detector and the surface. The measured kinetic energy of the emitted electron E_KE is

$$E_\mathrm{KE} = hv - E_\mathrm{B}, \tag{3.3}$$

where hv and E_B are the energies of the incident photon (hv_Mg = 1254 eV) and the involved bound electron state, respectively. Atom identification is possible using tabulated energies of the atomic bonds.

The thickness of the Al_2O_3 and interfacial oxide layers is calculated [3.10] from the measured XPS peaks A_Al, A_Si and A_SiOx by

$$t_\mathrm{AlOx} = -\ln\left(\frac{X_1 \cdot X_3 \cdot A_\mathrm{SiOx} + X_1 \cdot X_2 \cdot A_\mathrm{Si}}{X_2 \cdot X_3 \cdot A_\mathrm{Al} + X_1 \cdot X_3 \cdot A_\mathrm{SiOx} + X_1 \cdot X_2 \cdot A_\mathrm{Si}}\right) \cdot \lambda_1 \cdot \cos(\phi), \tag{3.4}$$

and

$$t_\mathrm{IL} = -\ln\left(\frac{X_2 \cdot A_\mathrm{Si}}{X_3 \cdot A_\mathrm{SiOx} + X_2 \cdot A_\mathrm{Si}}\right) \cdot \lambda_2 \cdot \cos(\phi), \tag{3.5}$$

respectively, where the X_i factors are $C_i \cdot S_i \cdot \lambda_i$. The correction factors X_i are determined by the attenuation length λ_i of the specific photoelectrons (e.g. Si 2p) in the material (e.g. SiO_2) [3.11,3.12], the pure element relative sensitivity factors S_i and a transmission correction C_i. The values in table 3.4 have been obtained by assumption of 4.00 g/cm^3 Al_2O_3 and 2.33 g/cm^3 Si, the geometry of the analysis system and measurements of reference samples.

		C [ ]	S [ ]	λ [nm]
X_1	Al	78.4	0.5735	2.5
X_2	Si	45	0.865	3.2
X_3	SiOx	82.9	0.865	2.9

Table 3.4: XPS parameters

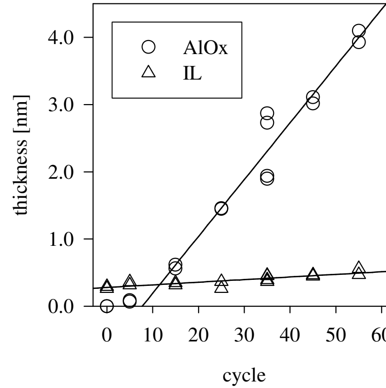

Figure 3.27: growth rate and interfacial oxide thickness as determined by angle resolved XPS measurements.

Figure 3.27 shows the growth rate and interfacial oxide thickness as determined by XPS measurements. The pairs of measurement points have been obtained from analysis at 0 and 45° angles. The growth rate is linear (0.0845 nm/cycle) during the steady state deposition of the layer, but this linear growth is retarded by 7-8 cycles. This growth rate agrees well with publications of other groups. [3.13–3.15] In the initial stage of some ALD processes, growth inhibition (or accelerated growth) is caused by the formation of the interface between substrate and deposited material. [3.16] However, the interfacial oxide layer does not significantly increase during deposition and is already present before the first ALD cycle. This means that the surface is oxidized during heating up to the deposition temperature.

More attention to the type of oxygen source is required, since this precursor oxidizes the silicon substrate and results in an interface layer. A high background concentration of H_2O (remaining precursor, from the N_2 source or vacuum leaks) results in an increased interface layer thickness. One improvement is the use of a more volatile precursor like O_3. An H-terminated (passivated) silicon surface has no active sites for metal precursors and thus an oxygen precursor is used as first reactant. Preferably, this first reaction is limited to a single (fully dense) layer of OH-terminated silicon atoms. An H-terminated Si(100) surface is to some extent passivated to adsorbed H_2O, but suffers from progressive oxidation above 380 °C. [3.17, 3.18]

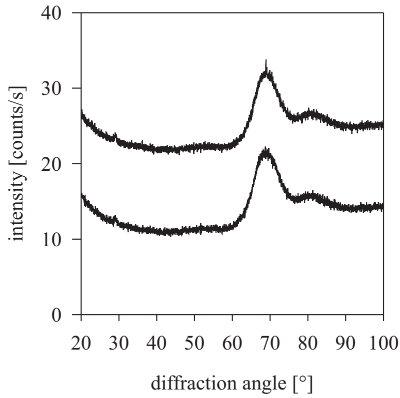

Figure 3.28: X-ray diffraction (θ-2θ) measurement of two samples show only peaks related to the silicon substrate.

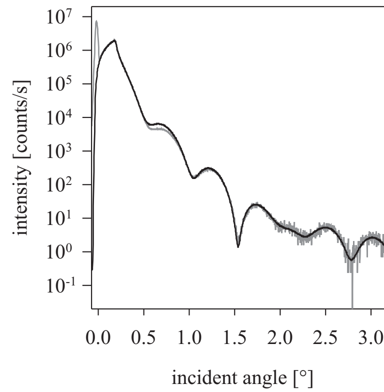

Figure 3.29: X-ray reflectivity results in a thickness of 9.2 nm and a density of 3.0 g/cm^3. The black line is the result of fitting the measurement data.

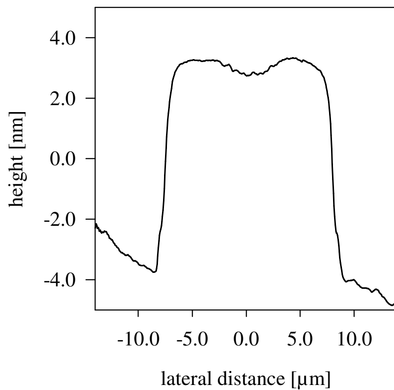

Figure 3.30: the step height of the etched Al_2O_3 layer (60 cycles) is about 7.0 nm.

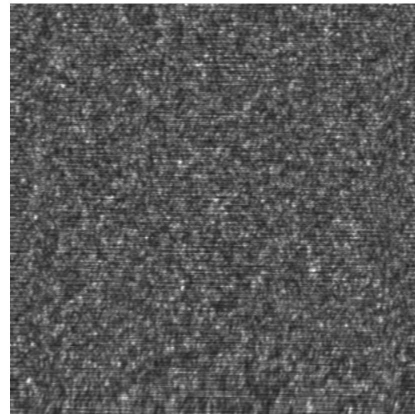

Figure 3.31: AFM image of the surface of the ALD Al_2O_3 layer (1×1 µm). The Z-range is 2.17 nm and the RMS surface roughness (R_q) of the scanned area is 0.24 nm.

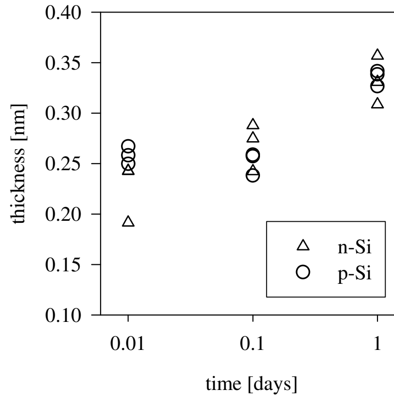

Figure 3.32: thickness of oxide layer after exposure to H_2O at 250 °C.

Figure 3.32 shows the measured oxide thickness after exposure to about 1 mbar H_2O vapor at 250 °C in the ALD reactor. The thickness was extracted from XPS measurements after transfer under vacuum conditions. Clearly, a disadvantage of H_2O as precursor is the unavoidable formation of an (interfacial) oxide layer before the ALD process starts. The interfacial oxide layer reduces the effective dielectric constant of the gate oxide stack (see equation 1.8 on page 14). However, the presence of an intermediate material avoids undesired intermixing (thermodynamic instability) as discussed in section 2.5. An ALD Al_2O_3 layer is therefore expected to show improved device characteristics when compared to the PLD Al_2O_3 layers.

Thin layers (100 cycles) have been investigated with X-ray diffraction (XRD) (Philips Analytical X'pert MPD PRO diffractometer) to identify the presence of crystalline phases and X-ray reflectivity (XRR) to determine the thickness and density of the layers. The only peak in the XRD results (3.28) of two samples originates from the silicon substrate. The thickness and density of the amorphous ALD layers is 9.2 nm and 3.0 g/cm^3, respectively. This density is considerably lower than the density of bulk α-Al_2O_3 (4.0 g/cm^3), which was assumed in the XPS thickness extraction. An acceptable fit to the XRR result was only obtained after including an interface layer and a surface layer (roughness) to the XRR software model.

An Al_2O_3 layer of 60 ALD cycles was partially etched by 1% HF and measured by AFM. The measured step height in figure 3.30 is about 7.0 nm, which is considerably higher than expected from figure 3.27. Figure 3.31 shows the

Figure 3.33: high resolution TEM cross-section of a gate stack with Al/TiW/TiN/Al_2O_3/SiO_x gate stack. The Al_2O_3 thickness is estimated to be 2.5 nm after 40 ALD cycles.

AFM image of the Al_2O_3 surface (before patterning), with a surface roughness of 0.24 nm. This value can be compared to the surface roughness of 0.63 nm for the 7.0 nm PLD Al_2O_3 layer (100 pulses in O_2) in section 2.3.3.

Although several techniques have been used to measure the thickness of the deposited Al_2O_3 layers, no effort was made to compare the different results and techniques in detail. Part of the deviation is intrinsic to the differences in measurement techniques (calibration, sensitivity, calculation model, etc.) and should be determined by measurement of a reference sample. A high resolution TEM cross-section is often used to confirm thickness measurements by other techniques. However, figure 3.33 shows that even with HRTEM it is difficult to extract a layer thickness in the nanometer range.

3.5 Conclusions

A custom-designed reactor was realized to study the ALD growth of high-κ dielectrics. The precursor transport by difference between vapor pressure and reactor pressure is likely to result in pulse times of several seconds. However, good estimates of the efficiencies of ALD chemistry and reactor design are required to predict the exposure times in an ALD reactor. Characterization of the reactor uncovered one important flaw in the design: the difference in power density and heated mass of the two (equally powered) heaters. In combination with the difficult location of the thermocouple feedback, the actual wafer temperature was estimated to be about 50 °C higher than the measured reactor temperature. This was confirmed by the CoSi experiments in section 3.3.2.

Several depositions with different pulse/purge times, reactor temperatures and pressures have been used to determine the ALD characteristics of the reactor. Variations in time by a factor 2.5, pressure by a factor 10 and temperature by 50 °C result in a more or less constant thickness. This is typical for ALD conditions, in which only the number of process cycles determines the thickness of the layer. The result is a best-known-recipe for deposition of Al_2O_3 in the ALD reactor: low pressure (0.1 mbar), 300 °C, 2.0 s precursor pulses and 5.0 s purge time. This (not very optimized) recipe gives uniform layers with a growth rate of about 0.085 nm/cycle in the linear region of the growth curve.

The different thickness measurement techniques (XPS, XRR, HRTEM, AFM, ellipsometry) give different results for layers deposited under supposedly similar conditions. Part of this difference is intrinsic to the difference in characterization techniques. The thickness extraction method used on XPS results is commonly used, but depends on the calibration of the system and

assumptions made in the layer model (e.g. density). Thickness measurement by AFM requires an etched step, it is a physical contact technique and can be easily biased by operator judgement. Other techniques exist, but are unfortunately usually not readily available. Without doubt, an in-situ characterization technique to monitor the deposition in real-time would be very welcome or interesting at least.

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Part III

Development

4 Electron reflection

The electron is the common particle that links deposition chemistry, material characterization, semiconductor device behavior, ..., and what not? A cloud of only a few electrons determine how atoms interact. Mobile electrons form an electric current, resulting in specific device characteristics. The well-known particle and wave properties of the electron allow interpretation of electron-solid interactions in various material characterization techniques. Finally, the electron can even be active during absence, leaving a vacant and mobile position called hole.

4.1 Introduction

Reflection high-energy electron diffraction analysis is based on information in the reflected and diffracted electron beams from the surface of a (crystalline) sample. A beam of high energy electrons (5 - 35 keV) is reflected off the sample surface at grazing incident angles, usually 1 - 3° with respect to the wafer surface. Similar to the reflection of light, Bragg's law describes the angle of incidence for constructive interference of electrons reflecting from lattice planes parallel to the sample surface. Bragg's law is written as

$$2 \cdot d \cdot \sin(\varphi) = n \cdot \lambda \quad n \in \mathbb{N}, \tag{4.1}$$

with λ the electron wavelength, φ the angle of incidence and d the distance between lattice planes.

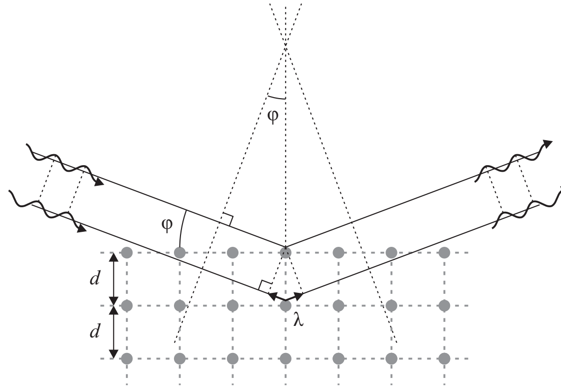

Figure 4.1: constructive interference according to Bragg's law.

The wavelength of the electron is related to its momentum by the "de Broglie" relation

$$\lambda = \frac{h}{p}, \tag{4.2}$$

in which p is the momentum and h is Planck's constant. In RHEED, the electrons are accelerated to a kinetic energy of $e \cdot V$, using an acceleration voltage V. Relativity theory describes the momentum of this acceleration as

$$p = \sqrt{2 \cdot m_e \cdot e \cdot V + \frac{(e \cdot V)^2}{c^2}}, \tag{4.3}$$

in which the fractional part is the relativistic correction. From equations 4.2 and 4.3 follows a wavelength of about 0.070 Å for 30 keV electrons. The angle of incidence in RHEED analysis is usually 1 - 3° with respect to the wafer surface. Equation 4.1 shows that for 30 keV electrons and a Si(100) surface (d = 5.43 Å), the diffraction order n is 3 - 8. Several Bragg diffraction angles are found in the range of grazing-incidence-angles used in RHEED.

The wavelength is a measure for the maximum resolution of the analysis, and should be in the same order as distance d. Therefore, X-ray diffraction with a wavelength of 1.54 Å (Cu K_α) is very suitable for analysis of the crystal lattice. Visible light has wavelengths in the range of 3500 - 6000 Å, resulting in the lower resolution of optical microscopy. [4.1] The wavelength of the electrons is considerably smaller than the size of and the distance between the scattering centers, i.e. atoms on (or near) the surface. Therefore, atomic features play a role in the diffraction and reflection of electrons on the surface.

In the initial stage of the ALD process, a low nucleation rate due to a low reactive sticking of precursors with the silicon surface is the cause of growth inhibition. [4.2] Characterization of this part of the deposition process is usually ex-situ [4.3] and at best without a vacuum break. [4.4] In situ monitoring of ALD with RHEED could provide direct growth information, contribute to growth model development and lead to improvement of device characteristics. Reflection high-energy electron diffraction (RHEED) is widely used for in situ analysis of (crystalline) growth in pulsed laser deposition (PLD) [4.5] and molecular beam epitaxy (MBE) [4.6] systems. Several ALD layers have been studied by ex-situ RHEED [4.7–4.9], although the photographs of the diffraction patterns are only presented to show (non)crystallinity of the deposited layers.

In this chapter the interaction between incident electrons and the sample surface will be discussed. This theoretical part will lead to expectations of the use of a RHEED analysis tool in an ALD process. The second part contains information on the implementation of the RHEED setup in the ALD reactor and the process of data acquisition. The last part presents the results obtained from in-situ RHEED measurements. Chapter 5 will use the results in a discussion on ALD growth modeling.

4.2 Electron-atom interactions

Lattice planes parallel to the surface are not the only source of constructive interference. In fact, all scattering centers (i.e. atoms) are source points of spherical wave fronts. Surface atoms in the same plane can therefore cause a diffraction beam, depending on the orientation of their periodicity with respect to the incident beam. In this section, the interaction of an electron with an atom will be quantified (under assumptions) to determine the effectiveness of electron diffraction in an ALD process.

4.2.1 Scattering potential

Incident electrons interact with the potential distribution around atoms, at and near the surface. This is different from X-ray diffraction in which incident X-rays interact with the charge distribution in the crystal. Both distributions are related by Poisson's second order partial differential equation

$$\varepsilon_0 \cdot \nabla^2 V(r) = -\rho(r), \tag{4.4}$$

with potential function $V(r)$ and charge density function $\rho(r)$, both as functions of the radial distance r. The effective range of the potential function is significantly larger than that of the charge density function, meaning that the effective size of an atom for electrons is larger than for X-rays. [4.10] Therefore, X-rays are more commonly used for crystal lattice analysis.

The scattering cross-section is roughly estimated from the Coulomb scattering potential of a single atom

$$V(r) = -\frac{Z \cdot e^2}{4\pi \cdot \varepsilon_0 \cdot r} \cdot \exp\left(-\frac{r}{a}\right), \qquad (4.5)$$

where Z is the atom number and a is the Thomas-Fermi screening length

$$a = \frac{4\pi \cdot \varepsilon_0 \cdot \hbar^2}{m_0 \cdot e^2 \cdot \sqrt[3]{Z}} = \frac{a_0}{\sqrt[3]{Z}}, \qquad (4.6)$$

and the Bohr radius a_0 = 0.529177 Å. [4.11] The screening length a of a silicon atom (Z = 14) is calculated to be about 0.22 Å. This is relatively small compared to the radius of the atom (1.10 Å), the Si-Si bond length (2.352 Å) and the distance between atoms in the Si lattice (2.70 Å). The scattering cross-section will be discussed in more detail in section 4.2.4.

4.2.2 Elastic scattering

The electron wavelength is much smaller than the size of atoms. Therefore, the interaction of electrons with the surface atoms in RHEED analysis should be described using wave mechanics. The momentum transfer of the incident wave with (propagation) vector $\boldsymbol{k}_0$ to an exit wave with vector $\boldsymbol{k}$, due to scattering on a surface atom (see figure 4.2), is $\hbar\boldsymbol{u} = \hbar(\boldsymbol{k} - \boldsymbol{k}_0)$. In elastic scattering, the amplitude of the exit wave vector is equal to the amplitude of the incident wave vector.

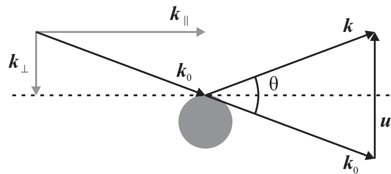

Figure 4.2: vector construction of incident and exit waves.

The reciprocal of the electron wavelength (and multiplied by 2π) is the amplitude of the wave vector $\boldsymbol{k}$, thus

$$|\boldsymbol{k}| = k = \frac{p}{\hbar} = \frac{2\pi \cdot p}{h} = \frac{2\pi}{\lambda}. \tag{4.7}$$

The wave vector amplitude of 30 keV electrons is about 900.29 nm^{-1}. Figure 4.3 shows the wave vector amplitude and the wave length as function of the kinetic energy.

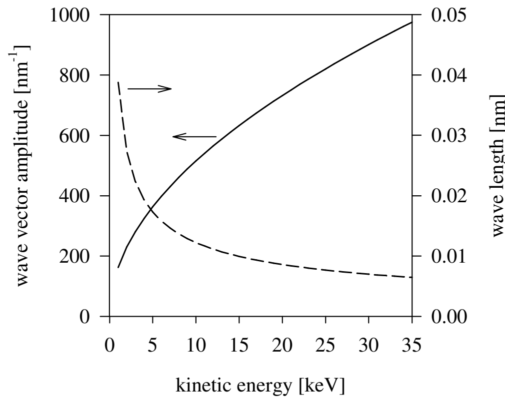

Figure 4.3: wave vector amplitude and wavelength of electrons.

4.2.3 Scattering amplitude

In the Born approximation, i.e. single atom scattering, the scattering amplitude is proportional to the Fourier transform of the scattering object. [4.11]

$$\begin{aligned} A(\boldsymbol{u}) &= -\frac{m_0}{2\pi \cdot \hbar^2} \cdot \mathrm{FT}[V(\boldsymbol{r})] \\ &= -\frac{m_0}{2\pi \cdot \hbar^2} \cdot \int_{-\infty}^{\infty} V(\boldsymbol{r}) \cdot \exp\left(-i \cdot 2\pi \cdot \boldsymbol{u} \cdot \boldsymbol{r}\right) \mathrm{d}\boldsymbol{r}. \end{aligned} \tag{4.8}$$

With a spherical symmetric atomic potential $V(\boldsymbol{r}) = V(r)$ and elastic scattering $|\boldsymbol{k}|^2 = |\boldsymbol{k}_0|^2$, equation 4.8 becomes

$$A(u) = -\frac{2m_0}{\hbar^2} \cdot \int_0^{\infty} V(r) \cdot r^2 \cdot \frac{\sin(2\pi \cdot u \cdot r)}{2\pi \cdot u \cdot r} \mathrm{d}r. \tag{4.9}$$

The scattering vector is defined as $\boldsymbol{s} = \boldsymbol{u}/2$ with amplitude

$$s = |\boldsymbol{s}| = \frac{2\pi \cdot \sin(\theta/2)}{\lambda} = k \cdot \sin(\theta/2), \tag{4.10}$$

and scattering angle θ. The scattering amplitude is usually expressed as a function of the scattering angle θ. Solving equation 4.9 results in the scattered amplitude

$$\begin{aligned} A(\theta) &= \frac{2m_0}{\hbar^2} \cdot \frac{Z \cdot e^2}{4\pi \cdot \varepsilon_0} \cdot \int_0^\infty r \cdot \exp\left(-\frac{r}{a}\right) \cdot \frac{\sin(S \cdot r)}{S \cdot r} \mathrm{d}r \\ &= \frac{2m_0}{\hbar^2} \cdot \frac{Z \cdot e^2}{4\pi \cdot \varepsilon_0} \cdot \frac{1}{S} \cdot \\ & \left[\exp\left(-\frac{r}{a}\right) \cdot \frac{\left(-\frac{1}{a} \cdot \sin(S \cdot r) - S \cdot \cos(S \cdot r)\right)}{S^2 + \left(\frac{1}{a}\right)^2} \right]_0^\infty \\ &= \frac{2m_0}{\hbar^2} \cdot \frac{Z \cdot e^2}{4\pi \cdot \varepsilon_0} \cdot \frac{a^2}{S^2 \cdot a^2 + 1}, \end{aligned} \tag{4.11}$$

with $S = 2\pi \cdot u = 4\pi \cdot s$ and scattering vector amplitude s as defined in equation 4.10. [4.11]

Elastic scattering amplitudes have been published in tabulated form for most elements in neutral and ionized state. [4.12] Figure 4.4 shows the scattering amplitudes for a few neutral atoms, as function of the scattering angle θ. In general, the scattering amplitude increases with atom number Z. Thus, silicon and aluminum have about the same scattering power. The scattered intensity from a single atom is calculated from its scattering amplitude

$$I(\theta) = |A(\theta)|^2 = \frac{4{m_0}^2}{\hbar^4} \cdot \frac{Z^2 \cdot e^4}{16\pi^2 \cdot {\varepsilon_0}^2} \cdot \frac{a^4}{(S^2 \cdot a^2 + 1)^2}. \tag{4.12}$$

4.2.4 Scattering cross-section

The scattered intensity $I(\theta)$ is a measure for the probability of scattering to an angle θ. The solid angle $\mathrm{d}\Omega = 2\pi \sin(\theta) \mathrm{d}\theta$ is used to define the change in impact area $\mathrm{d}A$ which results in scattering to the solid angle between θ and $\theta + \mathrm{d}\theta$. Integrating over all solid angles results in the total elastic scattering

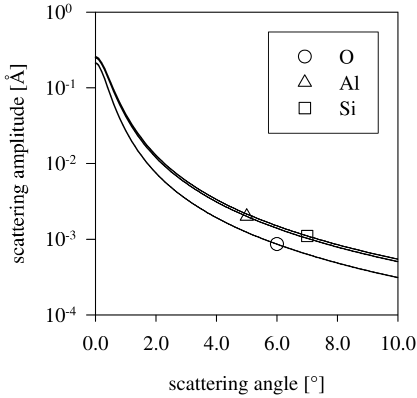

Figure 4.4: scattering amplitude $A(\theta)$ of a few neutral atoms as function of the scattering angle θ for 30 keV electrons.

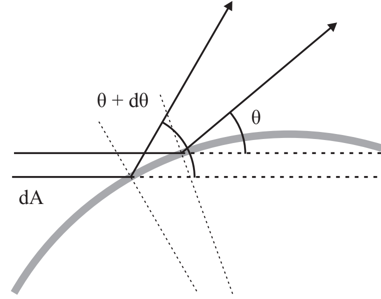

Figure 4.5: construction of the total scattering cross-section by integration of the scattered intensity over all angles.

cross-section [4.15], which represents the collision area of each of the atoms for scattering of incident electrons. With the solution of equation 4.12 the cross-section becomes [4.16]

$$\begin{aligned}
\sigma &= I(\theta)\,\mathrm{d}\Omega = 2\pi \int_0^{\pi} I(\theta)\cdot\sin(\theta)\,\mathrm{d}\theta \\
&= \frac{{m_0}^2}{\hbar^4}\cdot\frac{Z^2\cdot e^4}{2\pi\cdot{\varepsilon_0}^2}\cdot\int_0^{\pi}\frac{a^4\cdot\sin(\theta)}{(S^2\cdot a^2+1)^2}\,\mathrm{d}\theta \\
&= \frac{{m_0}^2}{\hbar^4}\cdot\frac{Z^2\cdot e^4}{2\pi\cdot{\varepsilon_0}^2}\cdot\frac{a^4}{k^2}\cdot\int_0^{2k}\frac{S}{(S^2\cdot a^2+1)^2}\,\mathrm{d}S \\
&= \frac{{m_0}^2}{\hbar^4}\cdot\frac{Z^2\cdot e^4}{2\pi\cdot{\varepsilon_0}^2}\cdot\frac{a^4}{k^2}\cdot\left[-\frac{1}{2a^2\cdot(S^2\cdot a^2+1)}\right]_0^{2k} \\
&= \frac{{m_0}^2}{\hbar^4}\cdot\frac{Z^2\cdot e^4}{\pi\cdot{\varepsilon_0}^2}\cdot\frac{a^4}{4\cdot k^2\cdot a^2+1}.
\end{aligned} \tag{4.13}$$

Figures 4.6 and 4.7 show the total elastic scattering cross-sections as function of the kinetic energy of the incident electron. The silicon atom has a cross-section of about 0.052 Å^2 (see table 4.1) for elastic scattering of 30 keV electrons. Figure 4.8 shows the scattering cross-section as calculated by equation

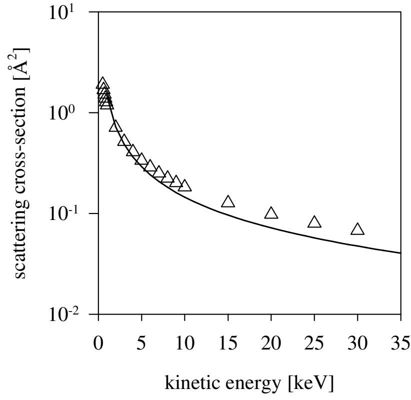

Figure 4.6: total elastic scattering cross-sections of an Al atom, calculated with equation 4.13 (lines) and results from [4.13] (symbols).

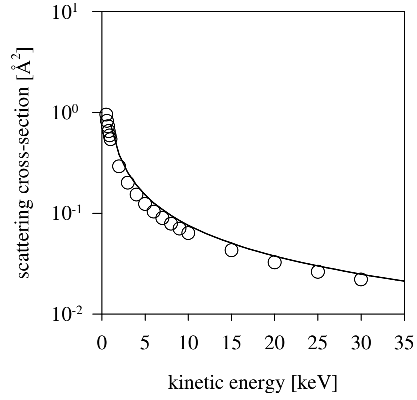

Figure 4.7: total elastic scattering cross-sections of an oxygen atom, calculated with equation 4.13 (lines) and results from [4.13] (symbols).

particle	scattering cross-section	ionization cross-section
Al	0.047	
Si	0.052	
H_2O	0.028	0.045
TMA	0.112	
N_2	0.042	0.051
CH_4	0.023	0.052

Table 4.1: scattering cross-sections and total ionization cross-sections [Å^2] of relevant particles for 30 keV electrons.

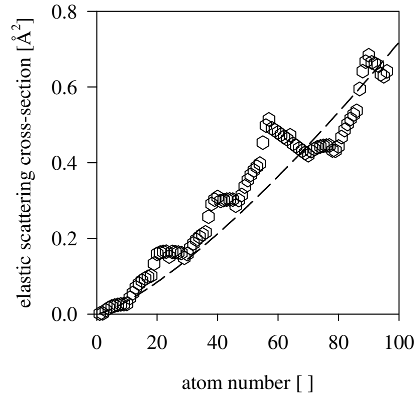

Figure 4.8: scattering cross-section for 30 keV electrons as calculated by equation 4.13 (line) and from the NIST database (symbols). [4.14]

4.13 (line) and as found in the NIST Electron Elastic-Scattering Cross-Section Database (symbols). [4.14]

4.3 Electron-solid interactions

The surface-normal component $\boldsymbol{k}_\perp$ of the wave vector $\boldsymbol{k}_0$ is small compared to the lateral component $\boldsymbol{k}_\|$ (see figure 4.2). A direct result is that the sampling depth of RHEED is very small, especially compared to the sampling area.

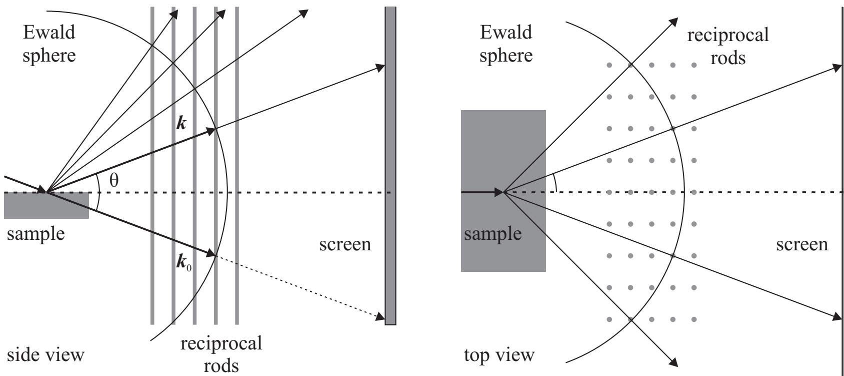

Figure 4.9: determination of diffraction beams using the Ewald sphere construction.

The periodicity of the sample lattice can be more easily visualized as its Fourier transformation. The Fourier transformation of the real space is called the reciprocal space, k-space, Fourier space or momentum space. The advantage of this transformation is that a lattice vector (in real space) is represented by a single point in reciprocal space. The vectors of periodicity in the two-dimensional lattice approximation result in a series of points in reciprocal space.

Approximating the sample by a two-dimensional layer, the reciprocal lattice becomes a set of 1-dimensional rods, perpendicular to the surface. A commonly used method to find the vectors of diffraction beams is the Ewald sphere construction. The Ewald sphere (see figure 4.9) is defined as a sphere around the origin of wave vector $\boldsymbol{k}$ (i.e. the point of incidence) with a radius $|\boldsymbol{k}|$. [4.17] The intersections of the Ewald sphere and the reciprocal lattice correspond to diffraction directions with maximum intensities. A periodic surface feature can be analyzed using RHEED, when the reciprocal lattice of the surface feature intersects with the Ewald sphere.

4.3.1 Crystal lattice

The potential distribution of a three-dimensional periodic crystal, i.e. the crystal potential, can be defined as the superposition of atomic potentials

$$V(\boldsymbol{r}) = \left(\sum_n \sum_\alpha V_\alpha(\boldsymbol{r} - \boldsymbol{r}_n - \boldsymbol{r}_\alpha)\right) \cdot S_\mathrm{p}(\boldsymbol{r}) \tag{4.14}$$

over infinite n unit cells and α atoms per unit cell. The crystal shape function S_p limits the crystal size to a finite number of unit cells in a 3-dimensional structure.

The scattering amplitude of the crystal is (again) the Fourier transform of the crystal potential [4.10]

$$\begin{aligned} V(\boldsymbol{u}) &= \mathrm{FT}[V(\boldsymbol{r})] \\ &= \left(\sum_n \sum_\alpha \int V_\alpha(\boldsymbol{r} - \boldsymbol{r}_n - \boldsymbol{r}_\alpha) \cdot \exp(-2\pi i \cdot \boldsymbol{u} \cdot \boldsymbol{r})\, \mathrm{d}\boldsymbol{r}\right) \otimes S_\mathrm{p}(\boldsymbol{u}) \\ &= \left(\sum_n \exp(-2\pi i \cdot \boldsymbol{u} \cdot \boldsymbol{r}_n) \cdot \right. \\ &\qquad \left. \sum_\alpha V_\alpha(\boldsymbol{u}) \cdot \exp(-2\pi i \cdot \boldsymbol{u} \cdot \boldsymbol{r}_\alpha)\right) \otimes S_\mathrm{p}(\boldsymbol{u}), \end{aligned} \tag{4.15}$$

which defines the crystal scattering power as a convolution of the Fourier transform of scattering centers with the reciprocal shape function $S_\mathrm{p}(\boldsymbol{u})$.

The reciprocal lattice is defined by vector $\boldsymbol{g}$

$$\boldsymbol{g} = (h \cdot \boldsymbol{a}^* + k \cdot \boldsymbol{b}^* + l \cdot \boldsymbol{c}^*), \tag{4.16}$$

which is constructed from the basis vectors of reciprocal space and the Miller indices (hkl). This reciprocal lattice vector is normal to the family of crystal planes $\{hkl\}$ and has a length of $1/d_{hkl}$. Thus,

$$\boldsymbol{g} \cdot \boldsymbol{r} = \boldsymbol{g} \cdot (n_1 \cdot \boldsymbol{a} + n_2 \cdot \boldsymbol{b} + n_3 \cdot \boldsymbol{c}) \in \mathbb{N} \quad n_1, n_2, n_3 \in \mathbb{N}, \tag{4.17}$$

where $\boldsymbol{a}$, $\boldsymbol{b}$ and $\boldsymbol{c}$ are the basis vectors of the unit cell (in real space). Reflections satisfy Bragg's law (see equation 4.1) in reciprocal space for $\boldsymbol{u} = \boldsymbol{g}$. Equation 4.15 now becomes

$$V(\boldsymbol{u}) = \left(\sum_g \delta(\boldsymbol{u} - \boldsymbol{g}) \cdot V_\mathrm{g}\right) \otimes S_\mathrm{p}(\boldsymbol{u}), \tag{4.18}$$

where V_g is the Fourier coefficient of the crystal potential

$$V_g = \frac{1}{\Omega}\sum_{\alpha} A(\boldsymbol{g}) \cdot \exp\left(-2\pi i \cdot \boldsymbol{g} \cdot \boldsymbol{r}_\alpha\right) \cdot \exp\left(-W_\alpha(g)\right), \tag{4.19}$$

where the last exponential is a correction for thermal vibration of atom α, called the Debye-Waller factor. [4.10] The Ω parameter is the volume of the unit cell and $A(\boldsymbol{g})$ is the electron scattering amplitude for atom α. Simplified, the diffraction pattern of an infinite (periodic) lattice of atoms is a convolution of the diffraction of a single atom with the reciprocal of the lattice.

The interaction of an electron beam with a sample in a RHEED system is actually more complex than described in this chapter. A complete account of the interaction of all electrons is not possible due to multiple scattering of electrons, inelastic scattering, crystal surface imperfections, dynamical effects, resonance reflections, mechanical vibrations, (electro)magnetic fields, geometry of RHEED screen vs Ewald sphere and temperature factors. Some of these effects result in the observation of streaks, Laue rings and Kikuchi patterns, instead of specific diffraction spots. The results of "RHEED analysis" are usually presented as photographs of a change in RHEED pattern, although more information may be obtained than a simple qualitative interpretation.

4.3.2 RHEED intensity

Summation over all scattering objects of interest, results in the scattering amplitude of electrons with the surface

$$A(\boldsymbol{u}) = \sum_{\boldsymbol{v}} f(\theta) \cdot \exp\left(-i \cdot \boldsymbol{u} \cdot \boldsymbol{v}\right). \tag{4.20}$$

The scattering *factor* $f(\theta)$ in this equation is the scattering *amplitude* of single atoms, as determined with equation 4.11. The real space vector $\boldsymbol{v}$ describes the distance from an arbitrary origin to the scattering atoms and consists of in-plane and layer-to-layer components. The latter is $|\boldsymbol{v}_\perp| = n \cdot d$, with interlayer spacing d and n an integer. The momentum transfer can also be split in parallel $\boldsymbol{u}_\parallel$ and perpendicular $\boldsymbol{u}_\perp$ components. Neglecting the scattering due to lateral distribution of atoms [4.18], equation 4.20 becomes

$$A(\boldsymbol{u}_\parallel = 0, \boldsymbol{u}_\perp) = \sum f(\theta) \cdot \exp\left(-i \cdot \boldsymbol{u}_\perp \cdot n \cdot d\right). \tag{4.21}$$

Interference of waves is constructive when their phase (shift) difference is less than half the wavelength. Maximum constructive interference occurs

where waves are exactly in phase. Combining Bragg's law with the wave vector amplitude, results in the momentum transfer for in-phase and out-of-phase conditions of electrons scattered from the top layer with electrons scattered from the underlying layer. The two conditions are set in equation 4.21, by substituting $\boldsymbol{u}_\perp$ with $2\pi/d$ or π/d respectively. The RHEED intensity is finally calculated as the square modulus of the scattering amplitude $I(\boldsymbol{u}) = |A(\boldsymbol{u})|^2$.

Based on the theory of electron diffraction, RHEED measurements during ALD are expected to start with a diffraction pattern of the single crystalline silicon substrate. Since all atoms should be considered as scattering centers, both gas phase molecules and chemisorbed precursor will affect the reflection and diffraction of electrons. The diffuse scattering on unordered atoms in an amorphous layer will reduce the intensity of the diffraction on the substrate. Diffraction spots and intensity oscillations of the diffracted beam(s) yield information on the growth mechanism. [4.17] Intensity oscillations, observed during epitaxial growth, have been related to the sequential completion of monolayers. [4.19] Specifically the intensity of the reflected (specular) electron beam is expected to provide valuable information on the growth process of (amorphous) layers in an ALD process.

4.4 RHEED setup and data analysis

In this section the implementation of the RHEED system will be presented, followed by an analysis of the limitations of the use of RHEED in an ALD process.

Small slits in the process chamber allow in situ RHEED analysis during deposition. The RHEED system is based on the high pressure RHEED setup used for PLD, [4.5] which can be used at relatively high process pressures (up to about 50 Pa). Figure 4.10 shows the hardware components of the RHEED setup.

A double differentially pumped STAIB Instrumente RH30DP electron source is used to generate a focused beam of (up to) 30 keV electrons. Diffraction (reflection) conditions are achieved by tilting the sample with respect to the electron beam and visualized using a fluorescent (phosphor) screen. The sampled surface area can be calculated from the electron beam diameter and

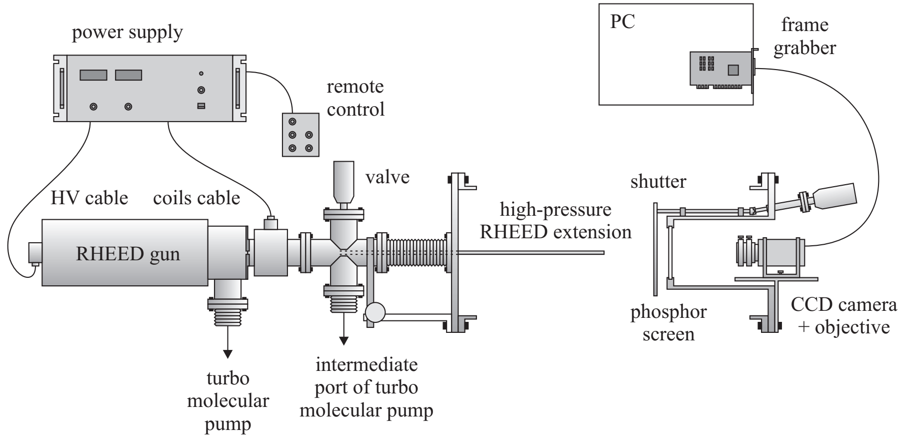

Figure 4.10: drawing of the hardware components for the RHEED setup.

the angle of incidence, using

$$\sin(\varphi) = \frac{w}{l} \tag{4.22}$$

$$A = \frac{\pi}{4} \cdot w \cdot l \tag{4.23}$$

where φ is the angle of incidence; w and l are the width and length of the elliptical projection of the beam on the surface, respectively. The diameter specification of a typical focused electron beam is 50 µm. An incidence angle of 1 - 3° results in a length l of 0.96 - 2.86 mm and an area A of 0.038 - 0.113 mm^2. This area contains about $2.6 \cdot 10^{11}$ - $7.7 \cdot 10^{11}$ surface atoms in the Si(001) plane, while the sampling depth is only a few monolayers. Figure 4.11 shows a cross-section of the deposition chamber and the maximum angle of reflection of the electron beam.

The intensity of the RHEED spot is recorded as 16-bit grayscale values from a 10-bit CCD camera (UNIQ UP-610, 110 fps, Sony ICX424AL progressive scan CCD, 659 × 494 pixels, 7.4 µm × 7.4 µm) with lens (Computar H6Z0812, 6× 8-48 mm F1.2), at a speed of about 64 fps. A single row and column of pixels represent lateral and longitudinal cross-sections of the reflected spot. This data is recorded, combined with the actual control signal of the precursor valves. Post-processing of the recorded information consists of fitting a (linear offset) Gaussian function, using a least squares optimization by Newton-Raphson iterations. This procedure is described in appendix B on page 153.

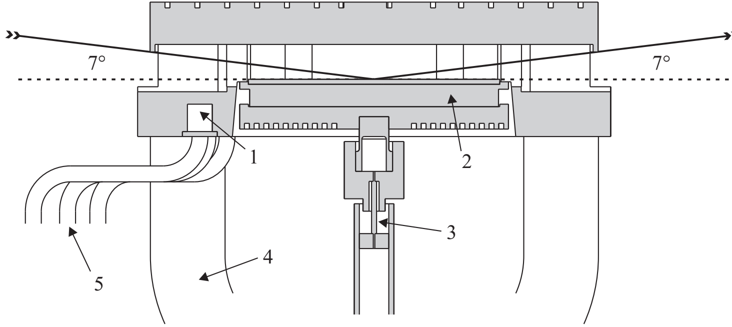

Figure 4.11: design of the angle of maximum RHEED reflection, with: 1. gas channel, 2. wafertray, 3. spring for tilt movement of process chamber, 4. gas outlet tubes, 5. gas inlet tubes.

The 3-parameter Gaussian function is combined with a linear tilt to form the 5-parameter function

$$I_G(x) = \frac{A}{C \cdot \sqrt{2\pi}} \cdot \exp\left(-\frac{1}{2}\left(\frac{x-B}{C}\right)^2\right) + D \cdot x + E, \tag{4.24}$$

with amplitude magnification A, average B, standard deviation C, tilt D and offset E. The full width of the peak at half its maximum ($FWHM$) is calculated from the standard deviation of the Gaussian

$$FWHM = \sqrt{8 \cdot \ln(2)} \cdot C \approx 2.355 \cdot C. \tag{4.25}$$

The fitting of the Gaussian function results in a few characteristic parameters, which can be more easily studied as a function of time. A disadvantage of this reduction of measurement data is the possible loss of relevant data or accuracy.

Figures 4.12 and 4.13 show the result of fitting the Gaussian function to a recorded row of 50 pixels. The extracted parameters become more accurate when both a horizontal and vertical cross-section is fit, e.g. using

$$\begin{aligned} I_G(x,y) &= \frac{A_{x,y}}{C_x \cdot C_y \cdot \sqrt{2\pi}} \cdot \exp\left(-\frac{1}{2}\left(\frac{x-B_x}{C_x}\right)^2 - \right. \\ &\qquad \left. \frac{1}{2}\left(\frac{y-B_y}{C_y}\right)^2\right) + D_x \cdot x + D_y \cdot y + E. \end{aligned} \tag{4.26}$$

Advanced image processing software could even take all recorded pixels into account to calculate the intensity of the RHEED spot.

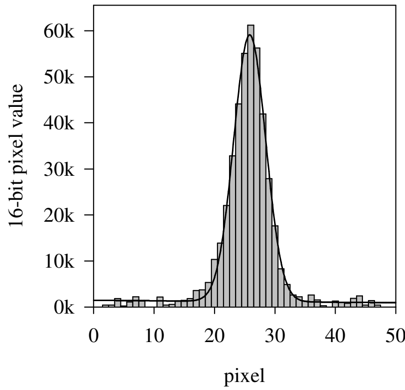

Figure 4.12: linear offset Gaussian function fit of the measurement data.

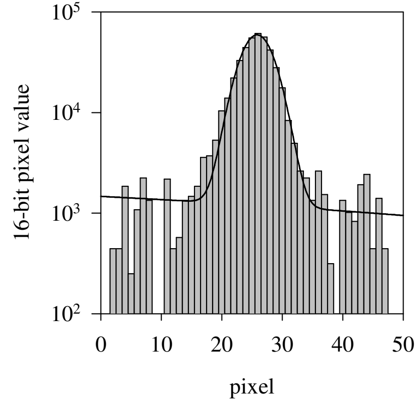

Figure 4.13: logarithmic scale graph of figure 4.12

The emission current of the electron beam is measured to be less than 0.01 µA, which is about $6.25 \cdot 10^{10}$ electrons per second. The amount of gas molecules n per volume V of ideal gas is calculated as

$$n = \frac{N_A}{R} \cdot \frac{p \cdot V}{T}, \tag{4.27}$$

with temperature T in K, pressure p in mbar and volume V in cm^3. The ratio of constants (Avogadro's constant N_A and gas constant R) is about $7.25 \cdot 10^{18}$ K/mbar cm^3. Water molecules have an effective cross-section of 0.045 $Å^2$ for 30 keV electrons (table 4.1). At 300 °C and 0.1 mbar pressure, an electron beam with a diameter of 50 µm and working distance of 150 mm will find $3.72 \cdot 10^{11}$ molecules in its path. These molecules have a total area of $1.67 \cdot 10^{-6}$ cm^2, which is about 8.5% of the area of the electron beam.

This rough estimation indicates that the pressure in the deposition chamber has a large impact on the electron beam. Figure 4.14 shows the recorded horizontal cross-sections and Gaussian fits of the direct focused beam at different N_2 pressures. The increase in pressure results in a reduction of the free path length of electrons. Figure 4.15 shows the attenuation of the direct beam intensity with pressure. Finally, the reactor pressure also affects the size (or FWHM) of the spot (see figure 4.16).

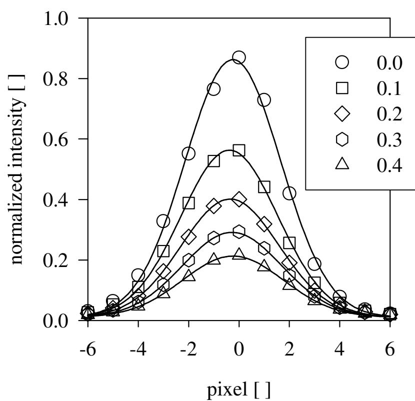

Figure 4.14: Gaussian fit of RHEED spot measured at different reactor pressures (in mbar).

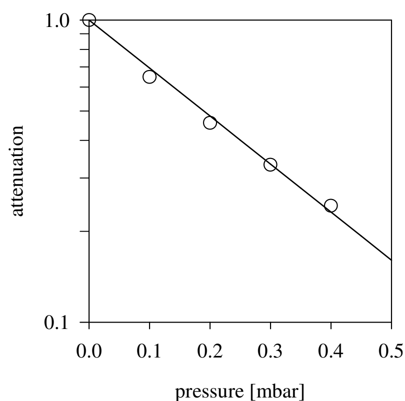

Figure 4.15: decay of RHEED intensity with pressure.

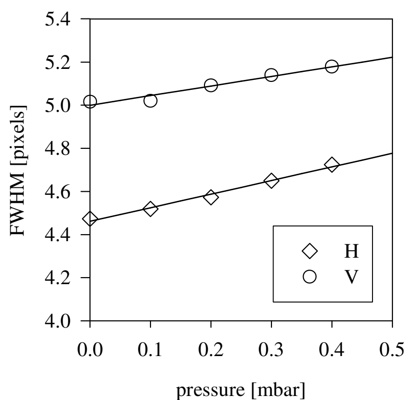

Figure 4.16: increase of spot FWHM with pressure, as determined from Gaussian fits of the horizontal (H) and vertical (V) cross-sections.

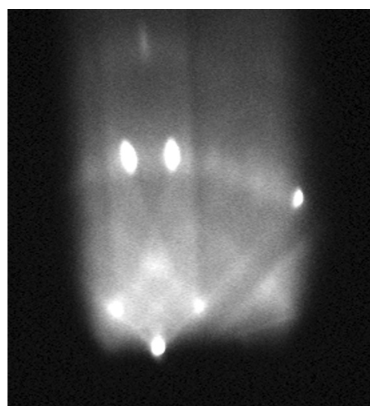

Figure 4.17: RHEED pattern of the bare silicon substrate.

4.5 Measurement results

Figure 4.17 shows a typical RHEED pattern of Si(001) in the [110] direction, as measured before deposition and before heating up to the deposition temperature. Most of the diffraction pattern is shadowed by the narrow slits in the gas block. The number of visible diffraction spots depends on the alignment of electron beam and process chamber (sample), with respect to the fluorescent screen.

Figure 4.18 shows the reduction in RHEED intensity for the first 20 ALD cycles. The vapor pressure of the various precursors determines the actual pressure in the reaction chamber. The mean free path of the high energy electrons at the pressures used, is smaller than the distance traveled in the reaction chamber. Therefore, the intensity of the signal depends on the changing gas composition in the ALD cycle. However, the purge steps after the H_2O and TMA pulses are identical in pressure and atmosphere, and are used as measurement windows.

The deposition of amorphous [4.20] Al_2O_3 results in the change of electron diffraction pattern to diffuse scattering. An additional variation of intensity is visible during every ALD cycle, before the signal is completely decayed. Figure 4.19 shows the intensity signal during 3 consecutive ALD cycles. The two binary signal lines in the top of figure 4.19 indicate the actual valve position of the two precursors. At the start of a purge step (at the closing of precursor valves) a rapid reduction and recovery of the intensity signal is observed. This is due to a high pressure burst of N_2 purge gas, intrinsic to the hardware used (figure 3.10), which reduces the mean free path of the electrons.

Figure 4.20 shows the effect of the reactive pulse (TMA or H_2O) on the intensity, based on the measured values during the purge steps. The change of intensity is calculated relative to the intensity level before exposure to the reactive pulse. Figure 4.20 also shows the ratio of the intensity changes due to TMA and due to H_2O exposure. This ratio appears to be a constant value after the first ALD cycle. The deviation of the first cycle is an indication of growth initiation by TMA, as reported by Frank. [4.21] Starting the ALD cycle by a TMA exposure, instead of a H_2O pulse, would result in a constant ratio of intensity changes.

The scattering cross section of neutral atoms is related to the electron scattering factor and the atom number. In the deposition of Al_2O_3 from TMA and H_2O, a model system for ALD high-κ oxides, only low numbered (light) atoms are used. Therefore, a change in electron scattering intensity [4.15] is expected

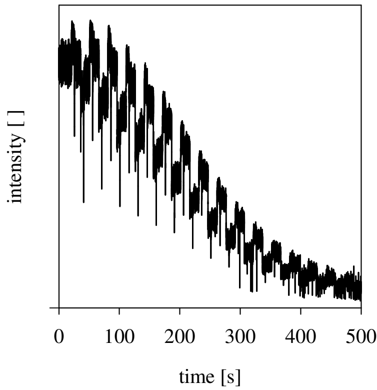

Figure 4.18: decay of RHEED intensity during the ALD process of Al_2O_3.

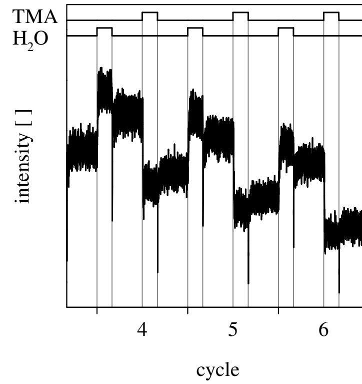

Figure 4.19: intensity change of the RHEED spot during 3 consecutive 30 s ALD cycles and its relation to the opened/closed (high/low) status of the precursor valves.

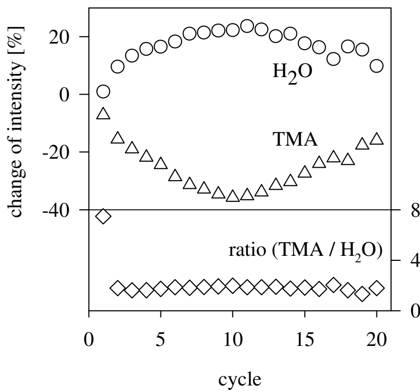

Figure 4.20: change in RHEED spot intensity due to the reactive precursor, as measured during the N_2 purge before and after the precursor pulse. Also, the ratio of changes in RHEED intensity due to TMA and due to H_2O exposure (TMA/H_2O).

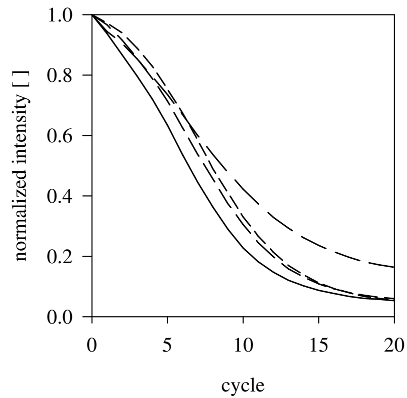

Figure 4.21: Intensity decay during repeated runs under supposedly same conditions.

to be not only due to a contribution of deposited aluminum atoms, but also to removal of precursor ligands.

The intensity signal reduces to its noise level in about 20 ALD cycles. The change in signal due to exposure to precursors is not always as strongly visible as in figure 4.20, even under apparently the same process conditions. This is probably caused by small differences in the angle of incidence of the electron beam. Figure 4.21 shows the intensity decay of repeat runs under supposedly the same conditions. A clear change in intensity of the signal was observed due to exposure to the reactive precursors. The decay in intensity due to (random) deposition of aluminum atoms was expected and will be faster when larger atoms are deposited. In general, the reduction in reflected intensity is related to an increase in surface roughness. The recovery of intensity due to exposure to H_2O is attributed to the removal of the methyl ligands, which is actually a reduction of surface roughness. The new hydroxylated bonding sites have a lower scattering power than the removed methyl groups.

4.6 Conclusions

The RHEED analysis technique was successfully implemented in an ALD reactor. The length between the high-pressure RHEED extension tip and the fluorescent screen (the travel distance of electrons in the high pressure region) is an important design issue. The experimental use of RHEED is limited by the free travel length of electrons and thus by the pressure. Other parameters that affect the RHEED pattern are the height, roughness and crystallinity of the surface. A very important focus point in the design should be the ability to achieve an accurately defined (and reproducible) angle of incidence.

An interesting signal was obtained from in-situ measurements during an ALD recipe. In general, the intensity of the specular reflected spot disappears to the noise level of the measurement in about 20 ALD cycles. In the deposition of amorphous layers, with increasing surface roughness, the intensity signal is not expected to increase again at some point in the deposition. The intensity changes due to TMA and due to H_2O exposure are caused by deposition of aluminum atoms and methyl ligands, and replacement of the ligands by OH-groups, respectively. The goal of the next chapter on ALD growth modeling is to find a more quantitative explanation for the measured RHEED signals.

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5 ALD modeling

By high school definition, a model is a simplified representation of reality. Well-known types of models, like fashion models and weather forecasting models, are usually wrong and should not be taken too seriously. Some scientific models allow the study of complex matter at an understandable level. The final question is usually on the validity of the model and how it should be modified to become more plausible.

5.1 Introduction

In a simple and commonly used deposition model, the solid-on-solid model (SOS) [5.1], a finite area is considered to be covered with cubic blocks in a close-packed array (see figure 5.1). The building blocks represent single atoms, molecules, unit cells or another unit of the deposited material. A set of basic deposition rules is used to define the preferential form of the deposition, resulting in different growth modes.

Nucleation of islands can be modeled by a set of rules which prefer growth on top of deposited material, instead of filling uncovered substrate positions. Layer-by-layer growth is modeled with rules which fill a layer completely before starting a new layer. The growth mode in an atomic layer deposition process depends on the deposited material, the used precursors, temperature and the type of substrate (termination). The ALD process of Al_2O_3 from TMA and H_2O on a H-passivated substrate has been identified to start with island formation. [5.2] Calculation of the change in RHEED intensity during an ALD process requires simplification of the electron-surface interaction. A continuous layer-by-layer growth model will be introduced in section 5.2. Modification to

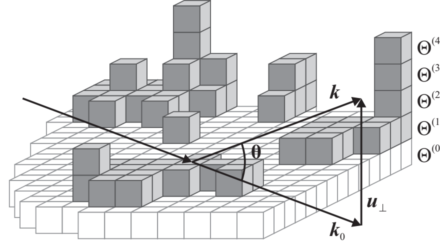

Figure 5.1: solid-on-solid surface model with wave vectors $\boldsymbol{k}$ and $\boldsymbol{k}_0$, and scattering angle θ. The deposited layers are $\Theta^{(n)}$ on substrate $\Theta^{(0)}$.

nonlinear growth (e.g. growth inhibition) forms the base for the ALD growth modeling in section 5.3.

5.2 Continuous growth

The layer coverage $\Theta^{(n)}$ is the total number of atoms in the nth layer divided by the total number of sites. In the solid-on-solid model of crystal growth, sites can only be occupied if the underlying site is occupied. The coverage of the nth layer $\Theta^{(n)}$ therefore depends on (and is equal or less than) the coverage of the underlying layer $\Theta^{(n-1)}$. So, the exposed surface fraction of the nth layer is

$$S^{(n)} = \Theta^{(n)} - \Theta^{(n+1)} \geq 0. \tag{5.1}$$

Assuming a time $\tau = 1$ is required to fill one layer, the growth rate is $\Delta\Theta = 1/\tau = 1$ layer per time unit. The model for layer-by-layer growth [5.3], e.g. epitaxial growth of silicon on silicon, can now be simply calculated per layer as

$$\begin{aligned}
\Theta^{(0)}(t) &= 1 \quad \text{completely filled substrate,} \\
\Theta^{(n)}(t) &= \begin{cases} 0 & t < (n-1)\cdot\tau \\ 1 & t > n\cdot\tau \\ \dfrac{t}{\tau} - (n-1) & \text{otherwise} \end{cases}
\end{aligned} \tag{5.2}$$

Recalling equation 4.21 for the scattering amplitude of electrons on the surface

$$A(\boldsymbol{u}_{\parallel} = 0, \boldsymbol{u}_{\perp}) = \sum_n f(\theta)\cdot\exp\left(-i\cdot\boldsymbol{u}_{\perp}\cdot n\cdot d\right), \tag{5.3}$$

and assuming full out-of-phase condition ($\boldsymbol{u}_\perp = \pi/d$) on visible blocks with scattering factor $f(\theta) = 1$, the amplitude becomes

$$A(t) = \sum_n S^{(n)}(t) \cdot \exp\left(-i \cdot \pi \cdot n\right) = \sum_n \pm \left(\Theta^{(n)} - \Theta^{(n+1)}\right). \qquad (5.4)$$

Figures 5.2, 5.3 and 5.4 show the linear completion of layer-by-layer growth, the surface fraction of each layer and the change in electron scattering intensity $I(t) = |A(t)|^2$. The roughness of the surface (figure 5.5) is calculated as the root-mean-square (rms) deviation from the average thickness $\Delta\Theta \cdot t$, using the surface fraction $S^{(n)}$ of all layers

$$R_{\mathrm{rms}}(t) = \sqrt{\sum_n S^{(n)} \cdot (n - \Delta\Theta \cdot t)^2}. \qquad (5.5)$$

The roughness changes from a flat surface ($R_{\mathrm{rms}} = 0$) to a half filled monolayer on top of a completely filled bulk ($R_{\mathrm{rms}} = 0.5$).

Assuming full constructive interference conditions ($\boldsymbol{u}_\perp = 2\pi/d$), the scattering amplitude becomes constant 1. This is simply because the full surface always consists of at least two stacked blocks (including the substrate) with full scattering factor. The in-phase condition becomes an interesting mode when layers have different scattering factors, due to different compositions of the building blocks.

The growth rate of a process which suffers from growth inhibition can be described as an exponential rise to a maximum growth rate, or

$$\Delta\Theta(t) = \alpha \cdot \left(1 - \exp\left(-\beta \cdot t\right)\right). \qquad (5.6)$$

The average thickness is derived from the growth rate

$$d(t) = \int_0^t \Delta\Theta(t)\,\mathrm{d}t = \alpha \cdot t - \frac{\alpha}{\beta} \cdot \left(1 - \exp\left(-\beta \cdot t\right)\right), \qquad (5.7)$$

in which the limit in growth rate is described by the linear function $\alpha \cdot t - \alpha/\beta$. The growth of layer n can now be described with the growth rate and the available surface fraction of that layer

$$\frac{\delta\Theta^n(t)}{\delta t} = \Delta\Theta(t) \cdot \left(\Theta^{(n-1)}(t) - \Theta^{(n)}(t)\right), \quad \Theta^{(0)}(t) = 1, \quad \Theta^{(n)}(0) = 0. \quad (5.8)$$

A general solution of this differential equation can be found by calculating a solution for the first layer from

$$\frac{1}{1 - \Theta^{(1)}(t)}\,\delta\Theta^{(1)}(t) = \Delta\Theta(t)\,\delta t, \qquad (5.9)$$

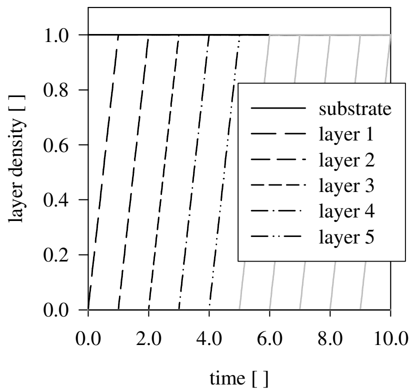

Figure 5.2: completion of layer-by-layer at a linear growth rate of 1 monolayer per time unit.

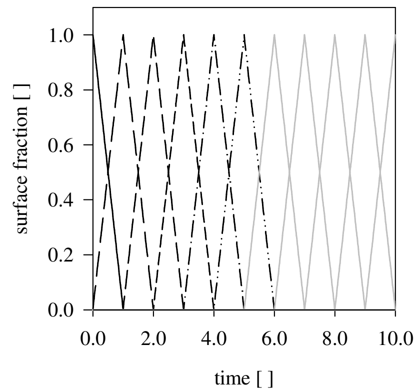

Figure 5.3: surface fractions of layers increase during completion and decrease during covering by the next layer.

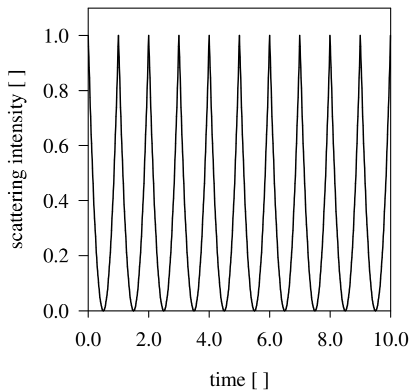

Figure 5.4: electron scattering intensity is maximum at completion of a layer and before starting the next.

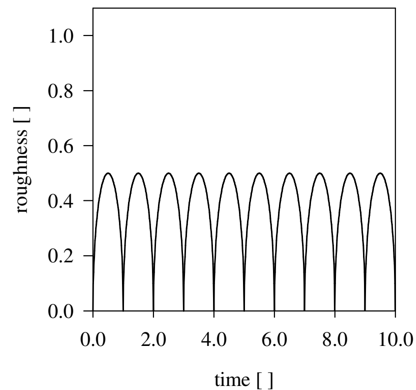

Figure 5.5: roughness of the surface changes between a flat surface and a half filled monolayer.

and using this solution to find a general equation for any layer n. Thus,

$$\begin{aligned}
\Theta^{(1)}(t) &= 1-\exp\left(-d(t)\right), \\
\Theta^{(2)}(t) &= 1-\exp\left(-d(t)\right)-d(t)\cdot\exp\left(-d(t)\right), \\
\Theta^{(3)}(t) &= 1-\exp\left(-d(t)\right)-d(t)\cdot\exp\left(-d(t)\right)-\tfrac{1}{2}d(t)^2\cdot\exp\left(-d(t)\right), \\
\Theta^{(n)}(t) &= 1-\exp\left(-d(t)\right)\cdot\sum_{j=0}^{n-1}\frac{d(t)^j}{j!},
\end{aligned} \tag{5.10}$$

in which $d(t)$ is the thickness function as described in equation 5.7. For the infinite layer $n\to\infty$, the summation in equation 5.10 becomes the Taylor series of $\exp\left(d(t)\right)$, and thus $\Theta^{(\infty)}(t)=0$.

The parameters in equation 5.6 can be obtained from the XPS measurements (figure 3.27) on ALD Al_2O_3 layers: α = 0.0845 nm/cycle and β = 0.129 cycle^{-1}. Normalized to a growth rate of 1 monolayer per time unit in the linear region of the inhibited growth, the graphs in figures 5.6, 5.7, 5.8 and 5.9 show the modeled growth of the layers and the expected electron scattering signal. The growth of layer 1 starts slowly, which is caused by the modeled growth inhibition. Immediately growth of layer 2 is started on the filled part of layer 1. This continuous growth quickly results in the surface composition consisting of all layers. The rapid decay of electron scattering intensity is directly related to the increasing surface roughness.

5.3 ALD modeling

The formation of islands by random deposition has been described using a discrete time model (ALD cycles), [5.4] similar to the birth-death time-domain models for epitaxial deposition. [5.3] In the latter model, the change in surface structure has been related to the electron scattering intensity of RHEED analysis, [5.5] although the scattering factor was simplified to unity. The inhibited growth is caused by the conversion of the substrate passivation to the required OH-terminated surface. Thus, the growth per cycle $\Delta\Theta$ changes from a low rate during interface formation to a higher rate during deposition of the bulk. The average growth in one cycle is calculated as a linear combination of both deposition rates,

$$\Delta\Theta=\Delta\Theta_{\mathrm{Si}}\cdot S_{\mathrm{Si}}+\Delta\Theta_{\mathrm{AlO_x}}\cdot S_{\mathrm{AlO_x}}, \tag{5.11}$$

with a ratio which is determined by the composition of the surface. [5.4] The sum of the surface fractions of substrate S_{Si} and deposited material $S_{\mathrm{AlO_x}}$, is

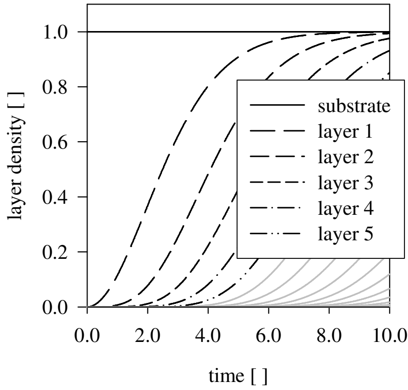

Figure 5.6: new layers start to be filled as soon as the sub-layer is being filled, i.e. deposition occurs in all layers.

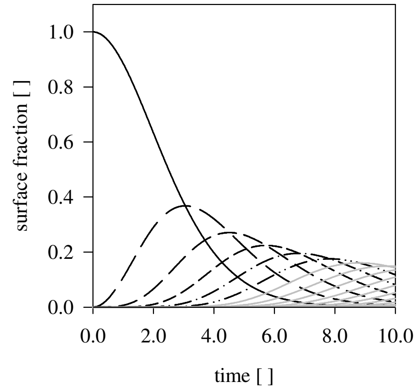

Figure 5.7: the surface composition consists of all layers.

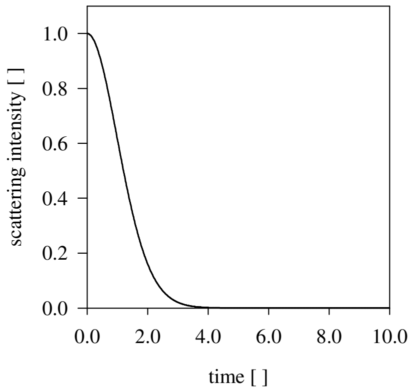

Figure 5.8: a rapid decay of electron scattering intensity is caused by the increase in surface roughness.

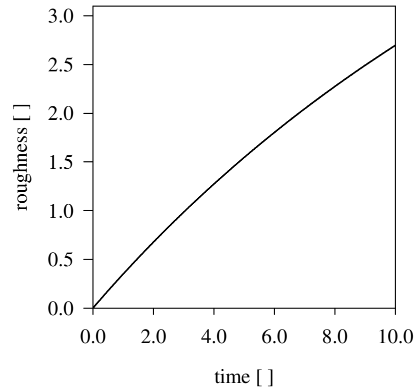

Figure 5.9: ever increasing surface roughness, since layers are never completely filled on an infinite surface.

unity for every ALD cycle $p = 1 \ldots P$. The surface fraction $S_p^{(n)}$ is the part of layer n which is not covered by layer $n+1$. The new surface fractions of layers $n = 0 \ldots N$ can be calculated using the growth per cycle in ALD cycle p

$$S_p^{(n)} = S_{p-1}^{(n)} + \left(\Delta\Theta_{\mathrm{Si}} \cdot S_{p-1}^{(0)} + \Delta\Theta_{\mathrm{AlOx}} \cdot (1 - S_{p-1}^{(0)})\right) \cdot \left(S_{p-1}^{(n-1)} - S_{p-1}^{(n)}\right). \quad (5.12)$$

The initial situation is an empty substrate $S_0^{(0)} = 1$, without deposited material $S_0^{(n)} = 0$ for $n > 0$ and the subsurface layers are fully covered by the top layer of the substrate $S_p^{(n)} = 0$ for $n < 0$. Including only scattering on blocks that form the top layer, equation 4.21 is changed to sum over all deposited layers

$$A_p = f_{\mathrm{Si}} \cdot S_p^{(0)} + f_{\mathrm{AlOx}} \cdot \sum_{n=1}^{P} S_p^{(n)} \cdot \exp\left(-i \cdot \boldsymbol{u}_\perp \cdot n \cdot d\right), \quad (5.13)$$

with their respective surface fractions $S_p^{(n)}$. Different scattering factors for the uncovered substrate f_{Si} and for the deposited material f_{AlOx} allows the model to differentiate between materials.

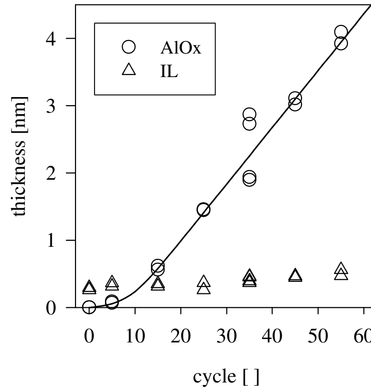

Figure 5.10: thickness measurements by XPS (under 0 and 45°) of the AlOx and interface layer after several ALD cycles. The line represents the growth curve for $\Delta\Theta_{\mathrm{Si}}$ = 0.025 and $\Delta\Theta_{\mathrm{AlOx}}$ = 0.355.

Figure 5.10 shows the results of thickness measurements by XPS of the deposited layer, as determined from the Al 1p peak. The samples have been transferred to the XPS without a vacuum break. A linear (least squares) fit of the measurement points of 15, 25, 45 and 55 cycles, results in a growth rate of $8.45 \cdot 10^{-2}$ nm/cycle.

With a monolayer thickness of 0.227 nm as determined by density functional theory (of close-packed O layers in crystalline α-Al_2O_3 and 5% expected increase for lower density amorphous layers) [5.6], the growth per cycle becomes 0.355 monolayers/cycle. The growth per cycle on the substrate $\Delta\Theta_{Si}$ = 0.025 monolayers/cycle is found by least squares fitting of the average thickness (accumulation of equation 5.11)

$$\bar{\Theta} = \sum_{j=0}^{J} \Delta\Theta^{(j)} \tag{5.14}$$

to the measured XPS data.

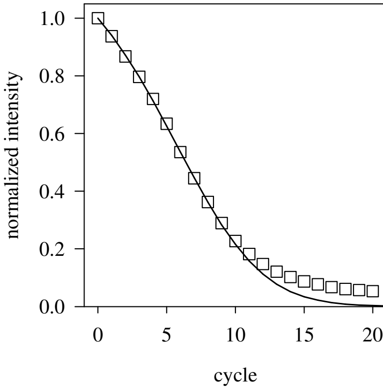

Figure 5.11: model fit (out-of-phase condition) of the intensity measured during the N_2 purge step after each ALD cycle.

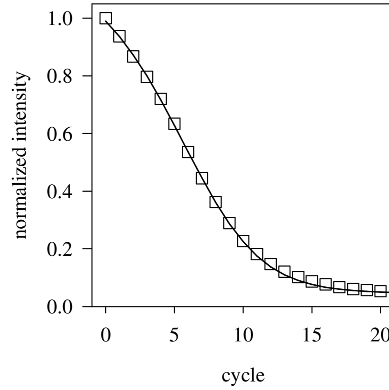

Figure 5.12: model fit (in-phase condition) results in a better fit near the end of the 20 cycle process.

Figures 5.11 and 5.12 show the measured intensity during the N_2 purge step after each ALD cycle. The line is the result of manually fitting the measured data by changing the growth per cycle values $\Delta\Theta_{Si}$ and $\Delta\Theta_{AlOx}$, and the scattering factors f_{Si} and f_{AlOx}. The results of both fits with their sum of squared errors can be found in table 5.1.

Figures 5.13, 5.14 and 5.15 show some results from the model with the parameters obtained in the in-situ condition: the increasing growth per cycle, the composition of the surface consisting of ever more layers and the increasing surface roughness. The three growth curves are compared in figure 5.16.

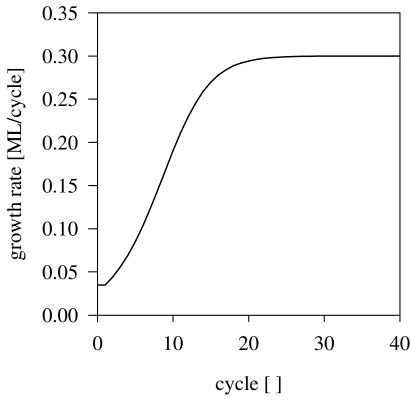

Figure 5.13: growth per cycle in the model with in-phase conditions.

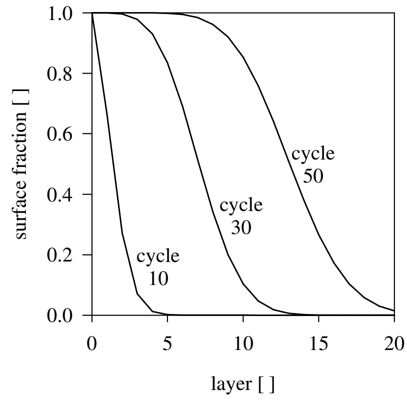

Figure 5.14: composition of the surface during ALD cycles 10, 30 and 50 (in-phase).

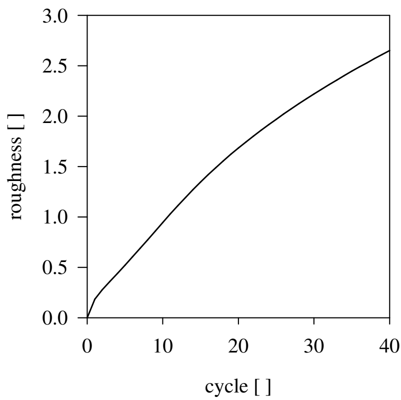

Figure 5.15: increase of surface roughness in the model with in-phase diffraction conditions.

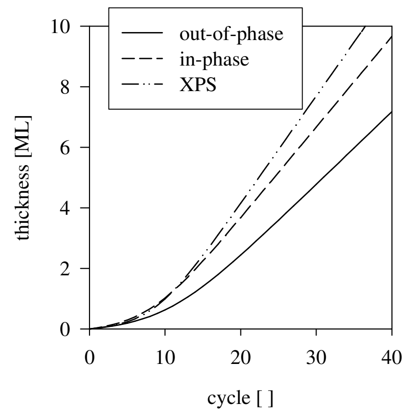

Figure 5.16: comparison of growth curves in the model (in-phase and out-of-phase) and based on the XPS results.

condition	out-of-phase	in-phase	XPS analysis
ALD cycles	0 - 10	0 - 20	15, 25, 45, 55
f_{Si}	1.0	0.99	1.0
$\Delta\Theta_{Si}$	0.025	0.035	0.025
f_{AlOx}	0.22	0.21	1.0
$\Delta\Theta_{AlOx}$	0.24	0.30	0.355
SSE	$3.1 \cdot 10^{-4}$	$2.0 \cdot 10^{-4}$	

Table 5.1: model parameters from fitting to the measurement data and the minimum sum of squared errors (SSE) of the fit. The last column shows the growth rates as obtained from XPS analysis (figure 5.10) as reference.

The intensity calculation in the growth model can be fit to the measured intensity, at least for the first 10 cycles. The intensity closely matches the measurement with $\Delta\Theta_{AlOx}$ = 0.24 - 0.30 monolayers/cycle and a scattering factor f_{AlOx} = 0.21 - 0.22. The average thickness after 20 cycles, as calculated from the model, is only 2.4 monolayers for out-of-phase conditions and 3.7 monolayers for in-phase scattering. The XPS thickness measurements (and the extracted growth per cycle values) indicate an average thickness of 4.1 monolayers after 20 cycles. The difference in growth per cycle found by XPS and RHEED should be attributed to model accuracy. Although island formation is included in the model, by different growth per cycle values on bare substrate and on deposited material, the random deposition mode omits some aspects of island formation.

Of all ALD cycles p, the odd and even cycles could be used to model exposure to TMA with scattering factor f_{TMA} and exposure to H_2O with scattering factor f_{H2O}, respectively. The change from modeling growth per cycle to modeling the exposure to each precursor, requires a modification to the growth model. Sequential exposure to the same precursor, without intermediate exposure to the second precursor, does not result in growth in the ALD chemistry. The ratio between scattering factors for TMA and H_2O is expected to be related to the measured ratio of change in intensity in figure 4.20. Although the model is time discrete and calculated as numerical series, fitting to the measurement data by iteration would result in more accurate results.

5.4 Conclusions

A discrete time model of ALD was used to analyze the measured decay in reflected intensity. The growth rate was modeled as a linear combination of

growth on the bare substrate and growth on the deposited layer. This way, growth inhibition was included in the model and a reasonable fit to the experimental results could be obtained. The obtained values for growth rates (0.24 - 0.30 monolayers/cycle on deposited aluminum oxide) differ from the experimental results, but are close enough to be applicable for rough estimations.

The source of electron scattering was assumed to be either completely in-phase or out-of-phase diffraction from the two topmost (visible) blocks on the surface. Basically, these two conditions form the extreme limits of an actual diffraction condition. The complete physics of electron scattering on a growing surface by ALD is far more complex than described and modeled in this chapter. The use of a scattering factor to correct for diffuse, multiple and subsurface layer scattering is too simplified to be of any practical use. Some directions for improving the model will be discussed in section 7.3.

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6 RF MOS analysis

The downscaling of transistors required huge efforts in the development of the semiconductor technology. However, the impact of this progress is not limited to the process technology and the functionality of the final product. Measurement systems and test methods have limited capabilities and accuracy. New analysis techniques are introduced to characterize the electrical behaviour of the ever shrinking stack of materials.

6.1 Introduction

The gate dielectric is, as explained in chapter 1, the critical part of the capacitor in a MOS field-effect transistor. An obvious electrical characterization technique is the capacitance-voltage measurement. Figure 6.1 shows three high-frequency C-V curves of ALD Al_2O_3 capacitors on the same wafer. The variation in thickness and area is due to TMA underdosing and wet etching of the aluminum contacts, respectively. However, the capacitors with the highest leakage currents suffer from a decreasing oxide capacitance in accumulation. This effect is caused by tunneling current through the dielectric layer and the series resistance of the device. [6.1–6.3] As a consequence, complicated device models have to be used to correct for this effect and allow extraction of device parameters.

A known solution to the influence of high leakage currents on capacitance-voltage characteristics is to increase the measurement frequency. This will be explained in the next section of this chapter. Results will be presented of capacitance-voltage characterization at radio frequencies (RFCV) on MOS

structures with ALD Al_2O_3 gate dielectric and ALD TiN metal gate. The MOS devices have been designed for the available process technology with 1.5 µm photolithography and to still be suitable for RFCV characterization.

The RFCV measurement methodology has been published for advanced sub-micron devices and nanometer thin dielectric layers. However, this measurement technique is not trivial on large scale devices with leaky oxide layers and the available measurement system. The work in this chapter is the result of collaboration with graduate students Adi Negara [6.4] and Mark Tiggelman [6.5]. The following sections will discuss the RFCV characterization technique, the design of the MOS devices and finally the results obtained.

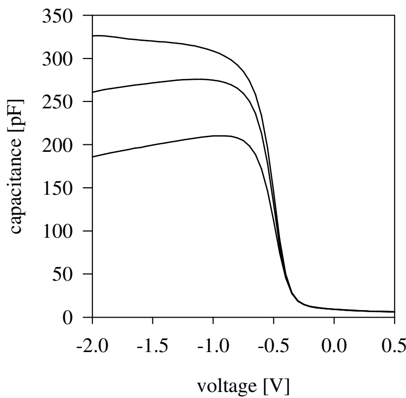

Figure 6.1: HF capacitance-voltage curves of ALD Al_2O_3 (25 cycles) capacitors, with variation in thickness and area due to TMA underdosing and wet etching of the aluminum contacts, respectively.

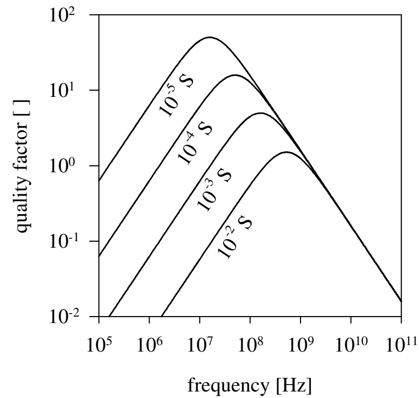

Figure 6.2: frequency dependence of the quality factor for different oxide conductance values (C_{ox} = 10 pF, R_s = 10 Ω).

6.2 RFCV characterization technique

The effects of leakage current through the gate dielectric on C-V measurements, can be analysed using the simple three-element model. The dielectric is modeled by a parallel circuit of a capacitance and a conductance. A series resistance completes the three-element model of a MOS stack in accumulation.

The impedance of the model is

$$Z = \frac{1}{i \cdot 2\pi f \cdot C_{\mathrm{ox}} + g_{\mathrm{ox}}} + R_{\mathrm{s}}. \tag{6.1}$$

The ratio of the imaginary part of this impedance to its real part, is a measure for the influence of the capacitance with respect to the oxide conductance and series resistance. The quality factor is

$$Q = -\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{2\pi f \cdot C_{\mathrm{ox}}}{g_{\mathrm{ox}} + R_{\mathrm{s}} \cdot (4\pi^2 f^2 \cdot {C_{\mathrm{ox}}}^2 + {g_{\mathrm{ox}}}^2)}. \tag{6.2}$$

The frequency dependence of the quality factor (see figure 6.2) shows a maximum value, which shifts to higher frequencies with increasing oxide conductivity. The reduction of the maximum quality factor due to leakage current through the oxide (see figure 1.6), emphasizes the importance of the measurement method to obtain accurate capacitance-voltage characteristics of thin dielectrics. [6.6, 6.7]
The maximum (optimal) quality factor

$$\max(Q) = Q_{\mathrm{opt}} = \frac{1}{2\sqrt{g_{\mathrm{ox}} \cdot R_{\mathrm{s}} \cdot (1 + g_{\mathrm{ox}} \cdot R_{\mathrm{s}})}}, \tag{6.3}$$

is obtained at measurement frequency

$$f_{\mathrm{opt}} = \frac{\sqrt{g_{\mathrm{ox}} \cdot R_{\mathrm{s}} \cdot (1 + g_{\mathrm{ox}} \cdot R_{\mathrm{s}})}}{2\pi \cdot R_{\mathrm{s}} \cdot C_{\mathrm{ox}}}. \tag{6.4}$$

Although an increase in measurement frequency could result in an improvement of the quality factor, the decreased wavelength approaches relevant dimensions of the measurement system. At that point, electromagnetic field theory should be applied and the measurement signal should be considered as traveling waves. Characterization measurements in the radio frequency (RF) range require a dedicated measurement setup, specific measurement and data processing techniques, and even special designed test structures on the wafer.

In RF capacitance-voltage characterization, the measurement setup behaves as a two-port transmission line system for traveling waves. The incident wave can be partly reflected on the port (i.e. one of the probes that contact the device under test) and partly transmitted to the other port, depending on the characteristic impedance of the system.

Scattering parameters (or S-parameters) are defined as the ratio of reflected and transmitted signal power, with respect to the power of the incident signal. The power reflected on the two ports ($|b_1|^2$ and $|b_2|^2$) is calculated from the incident power ($|a_1|^2$ and $|a_2|^2$), as

$$\begin{bmatrix} |b_1|^2 \\ |b_2|^2 \end{bmatrix} = \begin{bmatrix} |S_{11}|^2 & |S_{12}|^2 \\ |S_{21}|^2 & |S_{22}|^2 \end{bmatrix} \cdot \begin{bmatrix} |a_1|^2 \\ |a_2|^2 \end{bmatrix}. \tag{6.5}$$

The four scattering parameters are the impedances of the input and output port (S_{11} and S_{22}) and the forward and reverse transmission coefficients (S_{12} and S_{21}). The S-parameters are directly measured using a vector network analyzer (VNA) and can be converted to the well known Y (conductances) and Z (impedances) parameters for suitable device parameter extraction. [6.8, 6.9]

Accurate RFCV measurements require calibration of the measurement setup to compensate for the parasitic effects of cabling and probes. The short-open-load-thru (SOLT) calibration technique [6.10] is one of many calibration methods. A calibration sample is probed to measure the characteristics of a short circuit port, an open port, a well-defined $Z_0 = 50\ \Omega$ load and a direct connection between the two ports.

De-embedding is used to extract the intrinsic device properties from the (calibrated) device measurement. For this purpose, special structures are included to measure the parasitic effects of the probe pads and interconnect, which are also used to contact the device under test. A basic de-embedding technique for frequencies below 30 GHz, is the so-called open-short de-embedding procedure. [6.11] The intrinsic parameters of the device under test (DUT) are obtained from the Y-parameters of the three measurements (open, short and DUT). [6.12]

The complex Y_{11} parameter

$$Y_{11} = \frac{(1-S_{11}) \cdot (1+S_{22}) + S_{12} \cdot S_{21}}{(1+S_{11}) \cdot (1+S_{22}) - S_{12} \cdot S_{21}} = \frac{i \cdot 2\pi f \cdot C_{\mathrm{ox}} + g_{\mathrm{ox}}}{1 + R_{\mathrm{s}} \cdot (i \cdot 2\pi f \cdot C_{\mathrm{ox}} + g_{\mathrm{ox}})} \tag{6.6}$$

is used to extract the values of the three passive elements. (Note, the Y- and Z-parameters obtained from the measured S-parameters are normalized to the characteristic impedance Z_0 of the system.) The Y_{11}-based capacitance is approximately calculated as

$$C_{\mathrm{Y11}} = \frac{1}{2\pi f} \cdot \mathrm{Im}\{Y_{11}\}. \tag{6.7}$$

Alternative methods [6.13, 6.14] extract the capacitance by different calculation to eliminate specific parasitic components, which are not in the three-element model, e.g.

$$C_Z = \frac{1}{2\pi f} \cdot \mathrm{Im}\{\frac{1}{Z_{11} - Z_{12}}\}. \tag{6.8}$$

The values of the conductance g_{ox} and series resistance R_s are calculated as

$$R_s = \frac{\mathrm{Re}\{Y_{11}\}}{(\mathrm{Im}\{Y_{11}\})^2}, \tag{6.9}$$

and

$$g_{ox} = \mathrm{Re}\{Y_{11}\} - (2\pi f)^2 \cdot C^2 \cdot R_s. \tag{6.10}$$

Finally, the quality factor of the extracted capacitance value is

$$Q = -\frac{\mathrm{Im}\{Z_{11}\}}{\mathrm{Re}\{Z_{11}\}}. \tag{6.11}$$

6.3 Design of test structures

The design of the device structure can be optimized to allow the best possible measurement result (i.e. the highest quality factor). As indicated by equation 6.3, the series resistance of devices with leaky oxides should be minimized for an optimum quality factor. The series resistance in the three-element model is determined by both the gate and substrate side of the gate oxide.

The replacement of a traditional polysilicon gate by a metal gate, with its intrinsic lower resistance, offers a broader design margin for RFCV test structures. The gate resistance is calculated as

$$R_g \approx \frac{W}{3 \cdot L} \cdot \rho_{\square,g}, \tag{6.12}$$

in which the factor 1/3 is due to the distributed nature of the sheet resistance (from the edge to the center of the device). [6.15]

The series resistance (in accumulation) can be further reduced by creation of a well contact as close to the gate as possible. In the design of standard CMOS transistors, the distance between the well-contact and the gate is restricted by the location of source and drain implant regions on both sides of the gate. Assuming a distance L_s between the highly doped well contact and the gate, the effective well resistance is calculated as

$$R_w = \frac{L_s}{W} \cdot \rho_{\square,w}, \tag{6.13}$$

where $\rho_{\square,w}$ is the sheet resistance of the well (or substrate) below a source or drain implantation. A well-contact on both sides of the device reduces the resistance by a factor 2.

The use of dedicated test structures and a nonstandard CMOS process (all dopant implants prior to deposition of the gate stack), allows the design of a more optimized device. Since charge transport between source and drain is not of interest in RFCV measurements, a single source/drain implant on one side of the gate is sufficient to supply inversion layer charge to the substrate. This creates the possibility to place the well contact closer to the gate, even as close that the gate overlays the well contact implant region. In analogy with equation 6.12, the effective small-signal resistance of the inversion channel is

$$R_{\text{ch}} \approx \frac{L}{3 \cdot W} \cdot \rho_{\square,\text{ch}} = \frac{3 \cdot L}{W} \cdot \frac{1}{\mu_{\text{eff}} \cdot C_{\text{ox}} \cdot \left(V_{\text{gs}} - V_{\text{T}}\right)}. \tag{6.14}$$

The overall series resistance (and thus the quality factor of the C-V measurement) can now be calculated for the inversion ($R_g + R_{ch}$) and accumulation ($R_g + R_w$) regimes. With the typical values in table 6.1, the optimal quality factor (equation 6.3) is calculated as function of the gate width W. Figures 6.3 and 6.4 show that for both the inversion and the accumulation regime, a metal gate allows a very wide gate structure compared to a polysilicon gate. Also, a reasonable C-V measurement can still be obtained with a long channel structure. The capacitance value and quality factor should be sufficiently high ($C_{ox} > 1$ pF, $Q > 10$) to validate the extracted device parameters.

parameter	value (inversion)	value (accumulation)
$\rho_{\square,g}$	0.03 or 10 Ω/□	0.03 or 10 Ω/□
$\rho_{\square,ch}$	10 kΩ/□	n/a
$\rho_{\square,w}$	n/a	250 Ω/□
L	0.1 or 1.0 μm	0.1 or 1.0 μm
L_S	1.0 μm	1.0 μm
g_{OX}	1 MS/m²	1 MS/m²
C_{OX}	15 mF/m²	15 mF/m²

Table 6.1: values of the modelled RFCV structure with short channel (0.1 μm) or long channel (1 μm), and polysilicon or metal gate.

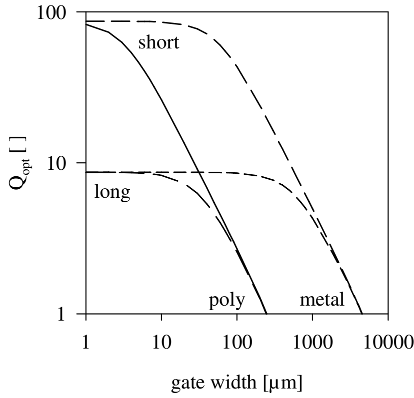

Figure 6.3: maximum quality factor Q_{opt} in inversion for short and long channel devices with poly or metal gates.

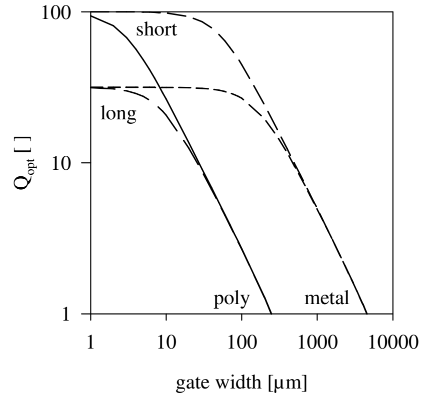

Figure 6.4: maximum quality factor Q_{opt} in accumulation for short and long channel devices with poly or metal gates.

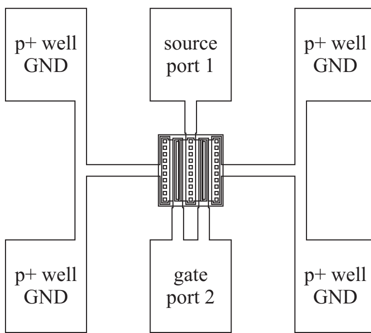

Figure 6.5: a 100/2 µm test structure for RFCV characterization.

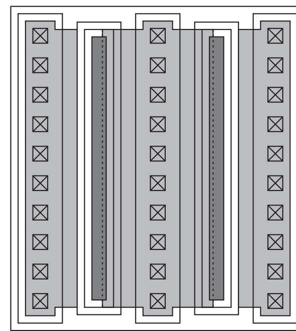

Figure 6.6: magnification of the actual device in figure 6.5, with gate oxide area (dark grey) and implanted regions (light grey).

6.4 Characterization results

Figures 6.5 and 6.6 show the designed test structures. The two-finger gate layout has limited effect on the already small contribution of the gate resistance to the overall series resistance. However, it yields some compensation for the photolithographic misalignment between the n^+ and p^+ implantation masks. The devices have been manufactured on 5-10 Ωcm p-type wafers with a p-well implant. The center implant region in figure 6.6 is n^+ doped, the outer two regions are p^+ well contacts. The gate stack consists of about 3.6 nm Al_2O_3 gate dielectric (50 cycles) with TiN/TiW/Al gate (see figure 3.33). The dielectric and TiN capping are both deposited by ALD, without an intermediate vacuum break.

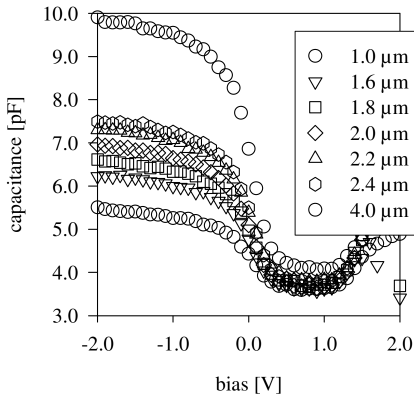

Figure 6.7: RF capacitance-voltage curves, obtained at 100 MHz from test structures with W = 100 µm and design rule λ = 2.0 µm.

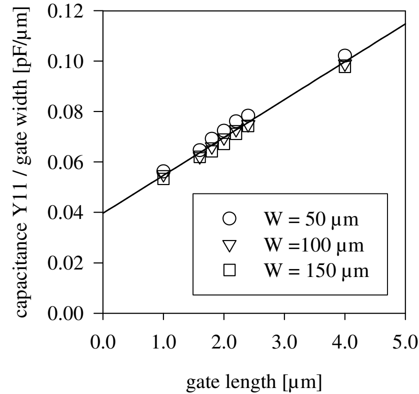

Figure 6.8: normalized Y11 capacitance in accumulation (-2.0 V) from measurements at 100 MHz.

The capacitance-voltage curves in figure 6.7 have been obtained from measurements at 100 MHz on test structures with W = 100 µm and design rule (scaling) λ = 2.0 µm. Figure 6.8 shows that the accumulation capacitance scales linearly with the W/L ratio. The intrinsic capacitance of the linear least squares fit is about 14.8 mF/m^2. This capacitance value corresponds to an equivalent oxide thickness (EOT) of 2.1 nm, which is higher than expected from the deposited Al_2O_3 layer (κ = 6.7) and the interfacial oxide layer.

Figures 6.9 and 6.10 show the capacitance-voltage curves of the shortest

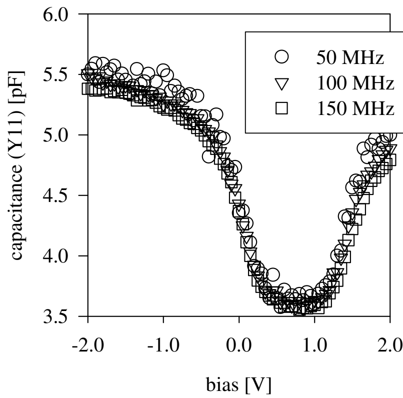

Figure 6.9: capacitance-voltage curves as obtained at three different frequencies and calculated with equation 6.7.

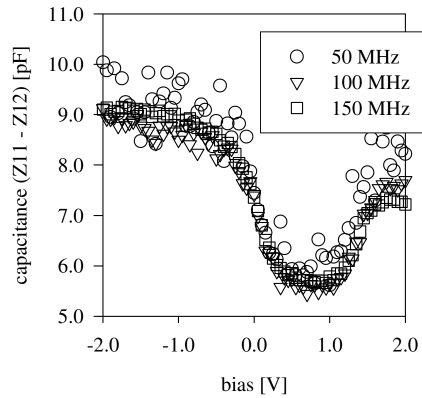

Figure 6.10: capacitance-voltage curves as obtained at three different frequencies and calculated with equation 6.8.

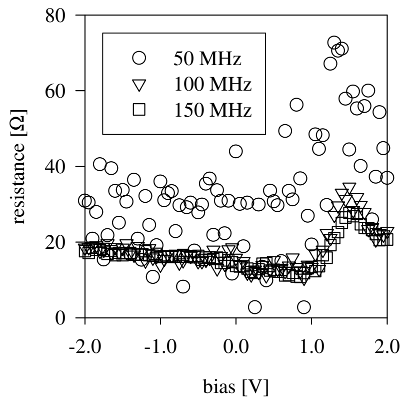

Figure 6.11: overall series resistance of the measured test structures.

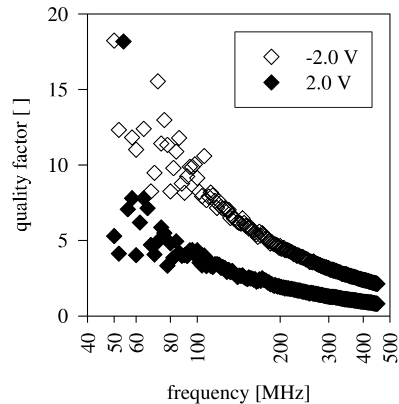

Figure 6.12: quality factors of the measured capacitance in inversion (2.0 V) and accumulation (-2.0 V).

channel (L = 1.0 µm, W = 100 µm) test structure. The capacitance values have been obtained with equations 6.7 and 6.8, respectively. The overall series resistance of the measured test structures is in the order of 20 Ω and is plotted in figure 6.11. The quality factor of the capacitance measurement has been calculated for the measured frequency range of 50 - 450 MHz. As expected from the curves of the modelled device (figures 6.3 and 6.4), the best quality factor is obtained in accumulation and at relatively low frequencies (see figure 6.12).

The differences between figures 6.9 and 6.10 induce questions on the correct method to extract the oxide capacitance from the measurement results. The intrinsic capacitance is part of the intrinsic impedance and calculated as

$$Z_{\mathrm{intr}} = \frac{1}{i \cdot 2\pi f \cdot C_{\mathrm{intr}} + g_{\mathrm{intr}}}, \tag{6.15}$$

in which g_{intr} is the intrinsic conductance of the oxide. The impedances of parasitic components between the gate and the n^+/p^+ regions (overlay), Z_{ov1} and Z_{ov2}, are calculated in the same way. The two remaining impedances, Z_{ch} and Z_{dep}, are different for inversion and accumulation and are modelled as either a capacitance or a resistance (see figures 6.13 and 6.14).

Using two Δ-to-Y transformations [6.8], the impedance circuit of figure 6.15 can be resolved to an equivalent, which is drawn in figure 6.16. The equivalent intrinsic impedance is found to be

$$Z'_{\mathrm{intr}} = \frac{Z_{\mathrm{intr}} \cdot Z_{\mathrm{ov1}} \cdot Z_{\mathrm{ov2}}}{Z_{\mathrm{intr}} \cdot (Z_{\mathrm{ov1}} + Z_{\mathrm{ov2}} + Z_{\mathrm{ch}} + Z_{\mathrm{dep}}) + (Z_{\mathrm{ov1}} + Z_{\mathrm{ch}})(Z_{\mathrm{ov2}} + Z_{\mathrm{dep}})}. \tag{6.16}$$

The Z-matrix of the circuit in figure 6.16 is

$$Z = \begin{bmatrix} R_{\mathrm{G}} + Z'_{\mathrm{intr}} + Z'_{\mathrm{dep}} + R_{\mathrm{well}} & Z'_{\mathrm{dep}} + R_{\mathrm{well}} \\ Z'_{\mathrm{dep}} + R_{\mathrm{well}} & R_{\mathrm{SD}} + Z'_{\mathrm{ch}} + Z'_{\mathrm{dep}} + R_{\mathrm{well}} \end{bmatrix}. \tag{6.17}$$

With $R_{\mathrm{G}} \ll Z'_{\mathrm{intr}}$ (metal gate), the subtraction $Z_{11} - Z_{12}$ in equation 6.8 results in the impedance Z'_{intr}.

Typically, the junction capacitance C_{j} is orders of magnitude larger than the sum of intrinsic and overlay capacitances. Combined with the generally low channel resistance R_{ch}, the impedance Z_{ch} can be safely ignored. The impedance Z_{dep} is part of equation 6.16 due to the gate overlap with the p^+ well contact. Assuming a negligible substrate resistivity R_{sub}, equation 6.16 simplifies to the parallel circuit of Z_{ov1}, Z_{intr} and Z_{ov2}

$$Z'_{\mathrm{intr}} = \frac{Z_{\mathrm{intr}} \cdot Z_{\mathrm{ov1}} \cdot Z_{\mathrm{ov2}}}{Z_{\mathrm{intr}} \cdot Z_{\mathrm{ov1}} + Z_{\mathrm{intr}} \cdot Z_{\mathrm{ov2}} + Z_{\mathrm{ov1}} \cdot Z_{\mathrm{ov2}}}. \tag{6.18}$$

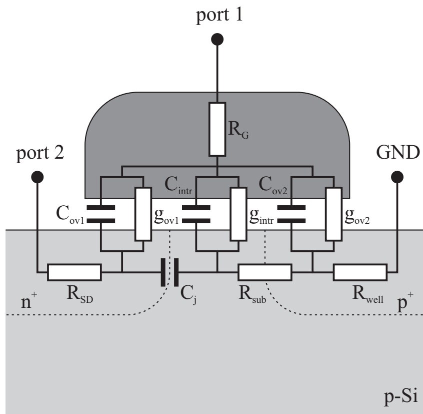

Figure 6.13: schematic of the RFCV test structure in accumulation.

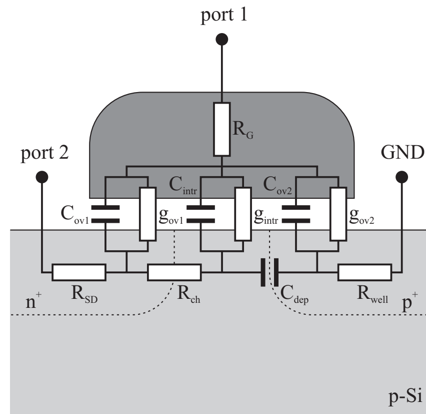

Figure 6.14: schematic of the RFCV test structure in inversion.

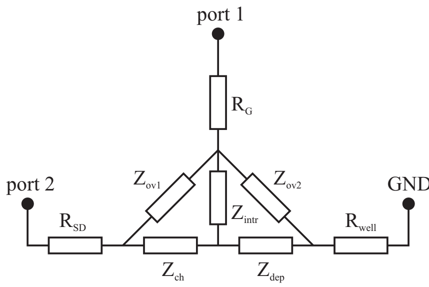

Figure 6.15: impedance circuit of the RFCV test structures in figures 6.13 and 6.14.

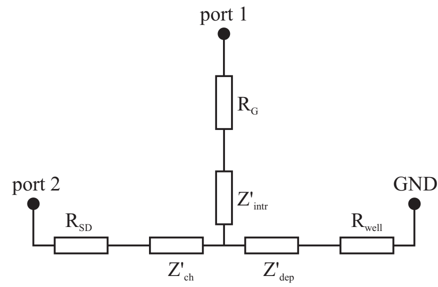

Figure 6.16: equivalent impedance circuit of figure 6.15, as obtained by Δ-to-Y transformations.

Under this obviously invalid assumption, the calculation by equation 6.8 [6.13] results in the oxide capacitance. On structures without the gate overlap of the p^+ well contact, the equivalent intrinsic impedance simplifies to the equation from which the solution for the oxide capacitance C_Z (equation 6.8) was obtained

$$Z'_{\text{intr}} = \frac{Z_{\text{intr}} \cdot Z_{\text{ov1}}}{Z_{\text{intr}} + Z_{\text{ch}} + Z_{\text{ov1}}}. \tag{6.19}$$

Finally, it should be mentioned that at high frequencies the charge carriers in the device may not be able to follow the applied signal. [6.16, 6.17] Non-quasistatic effects (NQS) can result in large deviations (e.g. additional channel resistance) when the measurement frequency is too high for the large lateral dimensions of the device. However, frequencies up to 500 MHz are considered to be still acceptable for the structures discussed in this chapter.

6.5 Conclusions

Electrical characterization of a thin dielectric layer suffers from high leakage currents, especially when a sub-micron process technology is not available and test structures can not be scaled laterally to match the thickness of the dielectric. A new test structure for RF capacitance-voltage characterization was designed, manufactured with a metal gate process technology and successfully tested. The results showed that the accumulation capacitance scales linearly with the designed gate dimensions. Capacitance-voltage curves can now be obtained from which device parameters (oxide thickness, flatband voltage, etc.) can be extracted.

The available methods for extraction of the oxide capacitance from the measurement are not suitable for devices in which the gate overlaps the p^+ well contact. However, the test structures without overlap are still expected to result in suitable C-V characteristics for device parameter extraction. The work in this chapter shows the direction for continued research on thin dielectrics with the available process technology and measurement setup.

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Part IV

Closing

7 Conclusions

The concluding part of a work is the indication of its end: the final result ... or whatever has been settled with. The contents of the conclusions basically consists of a recap and a verdict. The last sentence is finally terminated by a dot, maybe bold printed, but one that had wished to be an exclamation mark.

7.1 Summary

Since the introduction of the MOSFET transistor (metal-oxide-silicon field effect transistor) in 1960, the semiconductor technology underwent rapid development. This advancement consisted mainly of the capability to make transistors with ever decreasing dimensions and resulted in integrated circuits like the current Intel pentium 4 processor with 178 million transistors. The downscaling continuously improved not only the complexity and speed, but also for example the energy consumption and cost price, to become attractive to end users. While the current characteristic dimension of a MOSFET transistors is about 100 nm, this was a factor 100 larger about 30 years ago. By now, a number of physical limits have been reached and further development of the transistor is not possible without drastic changes to the production process.

The goal of this project was to contribute to the solution of an important barrier in the progress of semiconductor technology. Downscaling has resulted in a SiO_2 gate dielectric layer of only a few atomic layers thick. Electrons are able to tunnel through this layer at relatively low operating voltage, resulting in an unacceptable high energy consumption of chips. A solution can be found in the dielectric constant of the material: a higher dielectric constant allows

a thicker layer and thus a lower leakage current. However, the consequence is that the thermal oxidation process should be replaced by a deposition process. In the last few years, research has focused on the atomic layer deposition (ALD) technique to deposit thin dielectric layers. An example is the deposition of aluminum oxide Al_2O_3 from trimethylaluminum $Al(CH_3)_3$ and water H_2O.

The reflection high-energy electron diffraction (RHEED) technique allows analysis of the surface during deposition. Useful information on process and deposited material can be obtained from in situ RHEED measurements during ALD. This work shows the feasibility of using this surface sensitive analysis technique to study the surface chemistry during atomic layer deposition. A custom-designed reactor was realized to study the ALD growth of high-κ dielectrics. The results show the expected decrease in reflected intensity on deposition of aluminum atoms and methyl ligands. Also, a recovery of intensity was observed on exposure to H_2O. This recovery is attributed to removal of methyl from the surface. The observed intensity signal showed the growth initiation by TMA and the subsequent growth inhibition to last for more than 10 cycles. A discrete time model of ALD is used to analyze the measured decay in reflected intensity. Combining the information extracted from in situ RHEED measurements with ALD growth models, could result in model improvements and contribute to the proof of its validity.

7.2 Conclusions

The pulsed laser deposition technique was successfully used to deposit Al_2O_3 gate dielectrics from a single-crystalline sapphire target. Analysis of deposited layers by XPS, XRD, TEM, AFM, SEM and ellipsometry revealed the growth rate, stoichiometry and increasing surface roughness. Results of electrical characterization initiated a discussion about the high kinetic energy of ablated material and undesired surface reactions of deposited material.

A custom-designed reactor was realized to study the ALD growth of high-κ dielectrics. Characterization of the reactor uncovered one important flaw in the design: the difference in density and heated mass of the two (equally powered) heaters. Several experiments with different pulse/purge times, reactor temperatures and pressures resulted in a best-known-recipe for deposition of Al_2O_3 in the ALD reactor: low pressure (0.1 mbar), 300 °C, 2.0 s precursor pulses and 5.0 s purge time. This (not very optimized) recipe gives uniform layers with a growth rate of about 0.085 nm/cycle in the linear region. The different thickness measurement techniques (XPS, XRR, AFM, ellipsometry)

give different results for layers deposited under supposedly similar conditions. Without doubt, this motivates an in-situ characterization technique to monitor the deposition in real-time.

The RHEED analysis technique was successfully implemented in the reactor and diffraction conditions on a bare silicon surface could be obtained. An interesting signal was obtained from in-situ measurements during the first 20 cycles of an ALD recipe. The intensity changes due to TMA and due to H_2O exposure are caused by deposition of aluminum atoms and methyl ligands, and replacement of the ligands by OH-groups, respectively. However, obtaining a diffraction pattern and the interpretation of only a small visible part of it, is a challenging exercise but also a considerable limitation to the experimental potential of in situ RHEED.

A discrete time model of ALD was used to analyze the measured decay in reflected intensity. The growth rate was modeled as a linear combination of growth on the bare substrate and growth on the deposited layer. This way, growth inhibition was included in the model and a reasonable fit to the experimental results could be obtained. The obtained values for growth rates (0.24 - 0.30 monolayers/cycle on deposited aluminum oxide) differ from the experimental results, but are close enough to be applicable for rough estimations. The complete physics of electron scattering on a growing surface by ALD is far more complex than can be described in a model.

Finally, a new test structure for RF capacitance-voltage characterization was designed, manufactured with a metal gate process technology and successfully tested. The results showed that the accumulation capacitance scales linearly with the designed gate dimensions. Capacitance-voltage curves can now be obtained from which device parameters (oxide thickness, flatband voltage, etc.) can be extracted.

7.3 Recommendations

Further research on in-situ RHEED during ALD is necessary to determine its value in growth characterization. The ALD reactor described in this dissertation would require some drastic modifications to improve the experimental conditions. A few focus points and recommendations will be presented in this section.

First of all, the temperature control of the reactor should be changed (and calibrated) to determine the actual wafer temperature. Temperature overshoot during the upramp should be avoided by matching the power density of the two

heater elements to its thermal load. The two elements should be individually controlled by feedback from dedicated (local) thermocouples.

Oxidation of the silicon surface before exposure to the first precursor should be avoided. The main solution for this is to reduce the background concentration of water in the system by using high-purity (ultra dry) N_2. Additionally, switching from H_2O precursor to an O_2 plasma or O_3 and heating all walls of the reactor (above 300 °C) reduces the water concentration to a minimum. Literature reports on the formation of H_2O as byproduct from the reaction of O_3 with CH_3-ligands was not found. Even though, the required exposure and purge times for O_3 are shorter than for H_2O, due to the high chemical reactivity and less sticky nature of ozone. A related research topic is the use of an alternative surface termination of the starting material, e.g. chlorinated or methylated silicon surfaces.

Another focus point should be the ability to achieve an accurately defined (and reproducible) angle of incidence of the RHEED electron beam. The current design suffers from backlash during reversal of direction of the tilt mechanism and bending of the RHEED gun due to its weight. A more complete view of the diffraction pattern benefits the operation of the RHEED system and the analysis of the results. Mechanical vibrations from pumps and magnetic stray fields should be reduced or isolated from the RHEED system. Apparent solutions are readily available to solve vibration and stray field issues, but the should be included during the design phase of a system.

The described ALD growth model with electron scattering should be improved by using different scattering factors for exposure to TMA (f_{TMA}) and exposure to H_2O (f_{H2O}). Besides the change from modeling growth per cycle to modeling the exposure to each precursor, the model should exclude growth by sequential exposure to the same precursor, i.e. include the saturation density of each precursor. The variable material density during growth is expected to result in a more realistic model.

7.4 Original contributions in this work

- ◦ MOSFETs have been manufactured with Al_2O_3 gate dielectric deposited by pulsed laser ablation of a single-crystalline sapphire target.

- A custom designed experimental ALD reactor was realized in a cluster of two other reactors, XPS and AFM/STM analysis systems and a surface preparation chamber. Eventually, a sample could be transported

between all parts without a vacuum break.

- ◦ A RHEED analysis system was successfully implemented in the ALD system and diffraction conditions on a bare silicon surface could be obtained.
- The specular intensity of reflected electrons was measured during an ALD Al_2O_3 process.
- ◦ The observed changes in intensity during the ALD process have been related to changes in ambient pressure and the composition of the sample surface.
- A start was made with combining existing models for scattering intensity and ALD growth.
- ◦ The described model was used to compare the results of RHEED measurements with the XPS thickness measurements.
- A special structure for RFCV characterization of oxides in large devices was designed, manufactured and tested.

7.5 Publications of this project

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Samenvatting

(Abstract in Dutch)

In-situ RHEED en karakterisatie van ALD Al_2O_3 gate diëlektrica

Sinds de introductie van de MOSFET transistor (metaal-oxide-silicium veld-effecttransistor) in 1960, heeft de halfgeleidertechnologie een snelle ontwikkeling doorgemaakt. Deze vooruitgang bestond hoofdzakelijk uit de mogelijkheid om transistoren met steeds kleinere afmetingen te maken en resulteerde in geïntegreerde circuits zoals de huidige Intel Pentium 4 processor, waarop 178 miljoen transistoren te vinden zijn. Niet alleen de complexiteit en de snelheid, maar bijvoorbeeld ook het energieverbruik en de kostprijs, zijn door deze verkleining voortdurend verbeterd en daarmee voor de consument aantrekkelijk gemaakt. De karakteristieke afmeting van de MOSFET-transistor is nu ongeveer 100 nm, terwijl dat 30 jaar geleden nog een factor 100 groter was. Inmiddels zijn een aantal fysische grenzen bereikt en is een verdere verkleining van de transistor niet mogelijk zonder drastische aanpassingen van het productieproces.

Het doel van dit project was een bijdrage te leveren aan het oplossen van een belangrijke barrière in de vooruitgang van de halfgeleidertechnologie. Een van de belangrijkste onderdelen van de MOSFET-transistor is het gate-oxide. In de eerder genoemde ontwikkeling is het oppervlak steeds verkleind, met als gevolg dat het gate-oxide steeds dunner is geworden om voldoende capaciteit te behouden. Inmiddels heeft het gate-oxide echter een dikte bereikt van een tiental atoomlagen en kunnen elektronen al bij geringe spanning door het oxide tunnelen. Een materiaal met een hogere diëlektrische constante dan SiO_2

maakt het mogelijk om de laagdikte te vergroten en daarmee de lekstroom te verkleinen. Dit heeft echter tot gevolg dat het relatief eenvoudige thermische oxidatieproces vervangen moet worden door een depositieproces.

De laatste jaren wordt veel onderzoek verricht naar de zogenaamde atomic layer deposition (ALD) techniek, waarin door het sequentiële gebruik van gassen een gecontroleerde laag-voor-laag groei bereikt kan worden. Een voorbeeld van een ALD-proces, zoals toegepast in dit werk, is de depositie van aluminiumoxide Al_2O_3 door middel van trimethylaluminium (afgekort TMA) $Al(CH_3)_3$ en water H_2O. Met behulp van RHEED (reflection high-energy electron diffraction) is het mogelijk om tijdens de depositie het oppervlak te analyseren. In deze techniek wordt een elektronenbundel onder een kleine hoek via het oppervlak van de sample gereflecteerd en zichtbaar gemaakt op een fluorescerend scherm. In-situ RHEED kan nuttige informatie opleveren over de depositie in het ALD-proces. In dit onderzoek is een experimenteel clustersysteem gerealiseerd in de cleanroom van het $MESA^+$ Institute for Nanotechnology, bestaande uit o.a. een ALD-reactor met ingebouwd RHEED analysesysteem en een XPS analysesysteem.

De resultaten van RHEED analyse tonen de verwachte afname van gereflecteerde electronen door depositie van aluminiumatomen. De waterpuls veroorzaakt een herstel van de gereflecteerde intensiteit, door het verwijderen van methylgroepen van het oppervlak. De gemeten intensiteit toont groei-initiatie door de TMA-puls en de daarop volgende groeiachterstand gedurende meer dan 10 cycli. Een discrete-tijd model van ALD is gebruikt om de afname van de gereflecteerde intensiteit te analyseren. De combinatie van informatie uit in-situ RHEED metingen en ALD groeimodellen, kan leiden tot verbeteringen van een model en bijdrage aan het bewijs van geldigheid.

In hoofdstuk 1 wordt het onderzoek naar alternatieve diëlektrische materialen gemotiveerd. Hoofdstuk 2 bevat de resultaten van inleidend experimenteel werk, waarin Al_2O_3 lagen zijn gemaakt met behulp van de laserablatie techniek. De realisatie van de ALD reactor en de behaalde resultaten worden uitvoerig behandeld in hoofdstuk 3, gevolgd door het ingebouwde RHEED analysesysteem in hoofdstuk 4. In hoofdstuk 5 worden de resultaten van RHEED en XPS metingen met elkaar vergeleken, met behulp van een eenvoudig groeimodel. Tenslotte wordt in hoofdstuk 6 aandacht besteed aan de mogelijkheid om de elektrische eigenschappen van het oxide te karakteriseren met hoog frequente signalen en speciale test structuren.

Acknowledgements

Disclaimer: before reading the list of acknowledgements below, please be aware that due to unfortunate, unforeseen and unintentional circumstances your name may have suffered a (common) programming glitch, apparently resulting in typos or printing in white ink; the author is fully aware that you, as reader of this dissertation, have significantly contributed to this work and are therefore anonymously acknowledged; thank you.

First of all, I would like to thank the Dutch Technology Foundation STW for funding the project in which this work was realized. We have been very pleased with the investment in experimental equipment for long-term use in multiple (future) projects. The development of semiconductor technology by universities and research institutes was overtaken by the semiconductor industry. By enabling uncertain research directions in collaboration with semiconductor-related companies, valuable contributions to technology advancement can be expected.

For me, the project started immediately after my graduation assignment in the Semiconductor Components (SC) group. In retrospect, I value the confidence of Pierre Woerlee, Hans Wallinga and Jisk Holleman in my ability to complete this work. Although the relationship was somewhat reserved or distant, the freedom to define my own directions was very much appreciated. Jurriaan Schmitz joined the group after Pierre and Hans left the university and picked up the task of project leader with great enthusiasm. I want to cordially

thank Jurriaan and Jisk for their work in the project, their useful remarks on this dissertation and previous publications, and for taking the responsibility of promoter and assistant promoter.

A complete paragraph should be reserved to acknowledge the work, contributions, ideas, directions and friendship of Tom Aarnink. I will try not to forget the locations we had a few beers together: Enschede, Helsinki, Enschede, Seoul, ..., and probably Enschede a few more times. Perhaps with the exception of the trichloroethane incident, I have enjoyed working with and learning from you. Deservedly, you are considered the maternal father of the cluster tool.

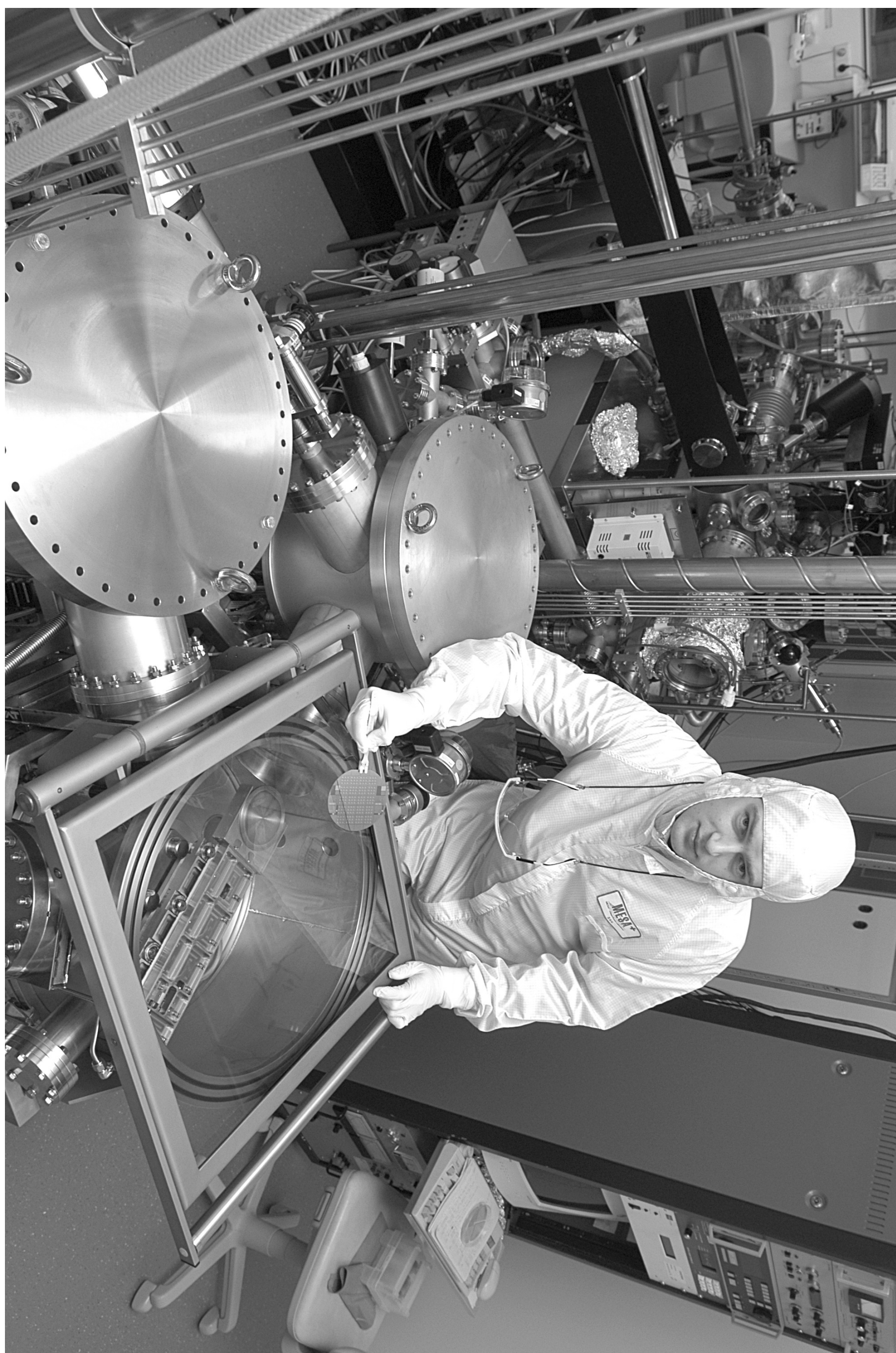
The cluster tool could not have been realized without the expertise, engineering and hard work of the guys at the Techno Center for Education and Research (TCO). Especially Peter Scheeren, Wilfried Raanhuis, Gert Niers, Lars van Tongeren, Rindert Nauta and André Eppingbroek are acknowledged for their work on hardware and software for this project.

Ofcourse, many many thanks to my students Adi Negara, Mark Tiggelman and Nguyen Van Toan, for making me think about things I should have been able to explain and their valuable contribution to the work presented in chapter 6 of this dissertation. I wish Toan all the best in running the lab at ITIMS in Vietnam; Mark and Adi the best of luck in their adventure towards their own PhD degree.

The project was a collaboration between SC and the Solid State Physics group of the faculty of Science and Technology. Bene Poelsema, Herbert Wormeester, Herman Oerbekke, Andrey Zinine and Marko Sturm are sincerely acknowledged for their involvement. The success of the collaboration was all about the development of the connection for sample transport under vacuum conditions, between the ALD reactors and the analysis tools. Andrey and Marko are also acknowledged for the results in figures 3.27 and 3.32.

I want to thank Frank Roesthuis for his kind assistance in the experimental work presented in chapter 2. Dave Blank, Guus Rijnders and Koray Karakaya are also acknowledged for their participation in the project. Rob Wolters is recognized for the idea of temperature calibration by cobalt-silicide formation and the reference measurements in figure 3.19. Albert van den Berg, Rico Keim and Mark Smithers are acknowledged for the XPS and TEM results on page 38 and in figures 2.3 and 2.4. Martin Siekman is thanked for his help in obtaining the nice AFM images on page 39.

Marcel Weusthof and Henk de Vries are sincerely thanked for their help with the measurement setups and electrical characterization issues. Thanks go



also to the staff of the MESA$^+$ cleanroom for their support and efforts to keep the tools up and running.

Sven Lindfors and Suvi Haukka are specially thanked for their valuable consultancy on ALD hardware and chemistry. Jan Willem Maes and Chris Rittersma are acknowledged for their input and time in the users' committee of the project. Valentin Aleskovskii and Riikka Puurunen are thanked for their kind remarks on the project website.

Finally, best regards and thanks to everybody on floor 3 for the coffee table conversations, the lunch break walks and other chit-chat.

And last but not least, I would like to thank my two sisterly paranymphs, Mirja and Sanja, for supporting me in the defense of this thesis and the difficult questions they may have answered.

Biography

Radko Gerard Bankras was born on November 30th 1975 in Bovenkarspel, The Netherlands. In 1994 he finished his preparatory scientific education at S.G. Oscar Romero high school in Hoorn, The Netherlands. Then he started his study Electrical Engineering at the University of Twente, Enschede, The Netherlands. From May to August 1999, he worked on nonvolatile memory in a standard CMOS process for Xilinx Inc., San Jose, USA. The results from this internship were rewarded by acknowledgement in US patent 6522582: "Non-volatile memory array using gate breakdown structures". On February 19th 2001, he presented the results of his graduation project for the chair of Semiconductor Components, entitled "Evaluation of nitridized TiW films for Cu diffusion barriers". In March 2001, he started working on the Ph.D. research project "Atomic layer CVD of high-κ metal oxides for MOS gate dielectrics" in the Semiconductor Components group. His educational task consisted of assisting students with the fabrication of photodiodes and test structures. The work in the Ph.D. project was interrupted from March to August 2004, to work temporarily as process support engineer for ASM Europe at Samsung Electronics Corp., South-Korea. In 2006, he completed his dissertation "In-situ RHEED and characterization of ALD Al_2O_3 gate dielectrics" and was employed by ASM Europe as process support engineer.

Appendix

A Diffusion barrier

The diffusion barrier is based on an inert blocking flow in opposite direction of the diffusing reactant. The speed of diffusion is found by solving the diffusion equation for a partial pressure gradient

$$\frac{\delta p_{\mathrm{r}}}{\delta t} = D \cdot \frac{\delta^2 p_{\mathrm{r}}}{\delta x^2}, \tag{A.1}$$

where $\mathrm{p_r}$ is the partial pressure of the reactant and D the diffusion coefficient. The solution of this differential equation for a constant source (worst case situation) is

$$\frac{p_{\mathrm{r}}(x,t)}{p_{\mathrm{r}_0}} = \mathrm{erfc}\left(\frac{x}{2 \cdot \sqrt{Dt}}\right), \tag{A.2}$$

where $\mathrm{p_{r_0}}$ is the partial pressure of reactant in the source and x the distance from the source. The boundary and initial conditions are

$$p_{\mathrm{r}}(x=0,t) = p_{\mathrm{r}_0}, \tag{A.3}$$

$$p_{\mathrm{r}}(x \rightarrow \infty,t) = 0, \text{ and} \tag{A.4}$$

$$p_{\mathrm{r}}(x \neq 0,t=0) = 0. \tag{A.5}$$

Note that the last condition defines an initially clean line. The speed of the diffusing reactant is the derivative of equation A.2

$$\frac{\delta x}{\delta t} = \sqrt{\frac{D}{t}} \cdot \mathrm{erfc}^{-1}\left(\frac{p_{\mathrm{r}}(x,t)}{p_{\mathrm{r}_0}}\right) = \frac{2D}{x} \cdot \left[\mathrm{erfc}^{-1}\left(\frac{p_{\mathrm{r}}(x,t)}{p_{\mathrm{r}_0}}\right)\right]^2. \tag{A.6}$$

Assuming the diffusing reactant should be blocked by a flow with speed v_b in opposite direction, the blocking distance x_b is

$$x_b = \frac{2D}{v_b} \cdot \mathrm{erfc}^{-1} \left(\frac{p_r(x,t)}{p_{r0}} \right)^2. \tag{A.7}$$

The velocity of the blocking flow is calculated as the volume flow F_b, divided by the cross sectional area of the gas line A.

level	$\mathrm{erfc}^{-1}()$
10^{-3}	2.3268
10^{-4}	2.7511
10^{-5}	3.1234
10^{-6}	3.4589
10^{-7}	3.7666
10^{-8}	4.0522
10^{-9}	4.3200

Table A.1: solution of inverse complementary error function, as calculated by Matlab.

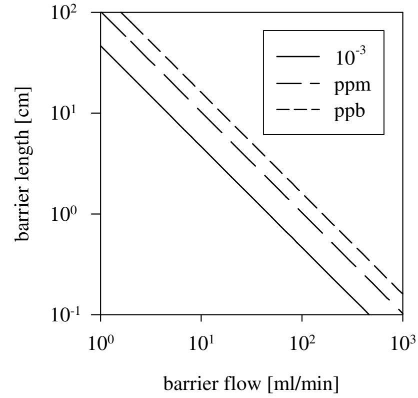


Figure A.1: required diffusion barrier length for H_2O precursor vapor at 293.15 K.

The diffusion coefficient of the reactant (in a gas ambient) is

$$D = D_0 \cdot \left(\frac{T}{T_0} \right)^{\frac{3}{2}} \cdot \left(\frac{p_0}{p} \right), \tag{A.8}$$

where D_0 is the diffusion coefficient at normal temperature and pressure, T_0 = 293.15 K and p_0 = 1 atm. The required length of the diffusion barrier is now calculated as

$$x_b = \frac{2 \cdot A \cdot D_0}{F_b} \cdot \left(\frac{T}{T_0} \right)^{\frac{3}{2}} \cdot \left(\frac{p_0}{p} \right) \cdot \left[\mathrm{erfc}^{-1} \left(\frac{p_r(x,t)}{p_{r0}} \right) \right]^2. \tag{A.9}$$

With a N_2 barrier flow of 50 ml/min and diffusing H_2O precursor vapor (figure 3.11: $D_0 = 22.6 \cdot 10^{-2}$ cm²/s), a diffusion barrier length of 3.2 cm (1/4 inch tube) is required for ppb-level at the end of the barrier. Figure A.1 shows the diffusion barrier length for 3 concentration levels, as function of the barrier flow.

B Gaussian fit

The intensity of the RHEED spot (see section 4.4) is recorded as 16-bit gray-scale values from a 10-bit CCD camera. A single row and column of pixels represent horizontal and vertical cross-sections of the spot. The recorded data is analyzed by fitting a 1-dimensional Gaussian function to either the row or column data. The 3-parameter Gaussian function is combined with a linear tilt to form the 5-parameter function

$$f(x) = \frac{A}{C \cdot \sqrt{2\pi}} \cdot \exp\left(-\frac{1}{2}\left(\frac{x-B}{C}\right)^2\right) + D \cdot x + E, \tag{B.1}$$

with amplitude magnification A, average B, sigma C, tilt D and offset E. The 5-parameter function is fitted to the discreet pixel data using a simple curve fitting algorithm, which is based on the Newton-Rhapson method for finding roots. The solution of the fit is the set of parameters which result in a minimum fitting error. This fitting error is the sum of the squares of the difference between the function and the pixel values. Thus

$$\sum_{k=1}^{N} \left(f(x_k) - p(x_k)\right)^2 \tag{B.2}$$

should be minimized, for a set $p(x_k)$ of N pixel values. This means that the roots have to be found of the derivatives of equation B.2 with respect to the 5 parameters.

$$F_i = \frac{\delta}{\delta a_i} \sum_{k=1}^{N} \left(f(x_k) - p(x_k)\right)^2 = \sum_{k=1}^{N} 2 \cdot \left(f(x_k) - p(x_k)\right) \cdot \frac{\delta f(x_k)}{\delta a_i} = 0 \tag{B.3}$$

where a_i is the set of parameters [A,B,C,D,E]. This set of functions is solved using a multidimensional version of the Newton-Rhapson method. The roots of a function $g(x)$ are found by iteration of

$$x_{n+1} = x_n + \frac{g(x_n)}{g'(x_n)} \tag{B.4}$$

for n steps until x stops changing (i.e. once g(x) = 0). The multidimensional version of equation B.4 is

$$a_{n+1} = a_n + \mathbb{J}^{-1}(a_n) \cdot F(a_n) \tag{B.5}$$

where a is the solution vector [A,B,C,D,E] and F the vector of functions for which the roots have to be found. Matrix $\mathbb{J}$ is the Jacobian of vector $F = [F_A, \ldots, F_E]$ and is defined as

$$\mathbb{J} = \begin{bmatrix} \frac{\delta F_A}{\delta A} & \cdots & \frac{\delta F_A}{\delta E} \\ \vdots & \ddots & \vdots \\ \frac{\delta F_E}{\delta A} & \cdots & \frac{\delta F_E}{\delta E} \end{bmatrix}. \tag{B.6}$$

The elements of the Jacobian matrix are calculated using equation B.3

$$\frac{\delta F_i}{\delta a_j} = \sum_{k=1}^{N} 2 \cdot \left[(f(x_k) - p(x_k)) \cdot \frac{\delta^2 f(x_k)}{\delta a_i \delta a_j} + \frac{\delta f(x_k)}{\delta a_i} \cdot \frac{\delta f(x_k)}{\delta a_j} \right]. \tag{B.7}$$

To find a suitable fit of function B.1 to the pixel data, the following steps are needed: find first and second order derivatives of the function to all 5 parameters, form the Jacobian matrix, calculate the inverse matrix $\mathbb{J}^{-1}$ and iterate until the solution is found. The inverse matrix of the Jacobian can be calculated using the Gauss-Jordan reduction method.

C Process flow

0. Starting material

wafer	size	doping	orientation	resistivity (Ω·cm)	dope (cm^{-3})
OSP	100 mm	B (p-Si)	<100>	5 - 10	10^{15}

1. Standard wafer cleaning (time: 30 min)

	step	time
1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 µS
4	boiling HNO_3 69% 110 °C	10 min
5	rinsing DI water	until conductivity < 0.1 µS
6	1% HF dip	until hydrophobic
7	rinsing DI water	until conductivity < 0.1 µS
8	spin dry	

2. Cleaning of oxidation furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	30
1100 - 800	-7.5	N_2	4	40

3. Growth of 25 nm pad oxide (time: 90 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 950	10	O_2 / $C_2H_2Cl_2$	2	15
950	-	O_2	2	30
950	-	N_2	2	20
950 - 800	-7.5	N_2	2	20

4. Ellipsometry of pad oxide (time: 10 min)

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
fixed	14.967	122.813	281.56	1.465	24.4

5. Flush LPCVD Si_3N_4 (time: 120 min) **WITHOUT WAFERS**

SiH_2Cl_2 (sccm)	NH_3 (sccm)	pressure (mTorr)	temperature (°C)	time (hours)
0	25	600	850	2

6. LPCVD of 50 nm Si_3N_4 (time: 60 min) **WAFERS IN CENTER**

SiH_2Cl_2 (sccm)	NH_3 (sccm)	pressure (mTorr)	temperature (°C)	dep. rate (nm/min)	dep. time (min:sec)
22	66	200	800	5	10:55

Comments: check recipe: fixed 01:00, variable 09:55

7. Ellipsometry of Si_3N_4 (time: 10 min)

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
float	23.449	72.796	178.77	2.004	48.04
fixed	23.449	72.796	178.31	2.008	47.99

Comments: Si_3N_4 on blanked wafer

8. Standard wafer cleaning (time: 30 min)
Comments: does not include HF etching

9. Photolithography of active area (mask AA) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
6000 rpm 20 s	1	3.6	1	45	NO

10. Plasma etching of Si_3N_4 (time: 5 min)

Phase 1 (descum)

O_2 (sccm)	pressure (µbar)	power (W)	matching network	time (s)
20	106	100	30/100	20

Phase 2 (etching Si_3N_4)

CF_4 / O_2 (sccm)	pressure (µbar)	power (W)	network	rate (nm/min)	time (min:s)
44	106	100	30/100	50	1:30

Comments: + 1 min. after rotation of wafers

11. Resist removal (time: 90 min)

step	O_2 (ml/min)	N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	60:00
4	0	500	0	01:00

12. Standard wafer cleaning (time: 30 min)

13. Cleaning of oxidation furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	35
1100 - 800	-7.5	N_2	2	40

14. Growth of 700 nm LOCOS field oxide (time: 4.5 hours)

temperature cycle (°C)	ramp (°C/min)	ambient	ambient temp (°C) tamson set-point	time (min)
800 - 1050	10	N_2/H_2O	85	25
1050	-	N_2/H_2O	85	200
1050 - 800	-7.5	N_2/H_2O	85	35

15. Ellipsometry of field oxide (time: 10 min)

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
fixed	81.655	98.974	281.56	1.465	699.27

16. Removal of oxidized Si_3N_4 (time: 15 s)

SiO_2 etch	etch rate	etch time (s)
HF / NH_4F 1:6	80 nm/min	15

17. Removal of Si_3N_4 (time: 20 min) **QUARTZ WAFER CARRIER**

Si_3N_4 etch	etch rate	temperature	etch time (min)	overetch (min)
H_3PO_4 85%	3.5 nm/min	180 °C	15	5

Comments: extra etch time, 30 min total

18. Standard wafer cleaning (time: 30 min)

19. Etching of pad oxide (time: 2 min)

SiO_2 etch	etch rate (nm/min)	etch time (min)
1 % HF	8	3

Comments: + 30 s overetch

20. Cleaning of oxidation furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	30
1100 - 800	-7.5	N_2	2	40

21. Growth of 25 nm sacrificial oxide (time: 90 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 950	10	O_2 / $C_2H_2Cl_2$	2	15
950	-	O_2	2	30
950	-	N_2	2	20
950 - 800	-7.5	N_2	2	20

22. P-well implantation (time: 90 min)

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	mass (amu)	2nd magnet (A)
B^+	$1.5 \cdot 10^{13}$	8.00	350	11 (10.81)	10.7
B^+	$4.0 \cdot 10^{12}$	2.13	110	11 (10.81)	5.7
B^+	$2.0 \cdot 10^{12}$	1.07	40	11 (10.81)	3.7

23. Standard wafer cleaning (time: 30 min)

24. Cleaning of annealing furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	35
1100 - 800	-7.5	N_2	2	40

25. Removal of lattice damage (time: 120 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800	-	N_2	4	30

26. Photolithography of implantation mask (mask SD) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
3000 rpm 20 s	1	6.0	1	45	**30**

27. Implantation of S/D regions (time: 90 min)

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	mass (amu)	2nd magnet (A)
As^+	$2 \cdot 10^{15}$	1067	100	75 (74.92)	15.5
P^+	$5 \cdot 10^{13}$	27	70	31 (30.97)	8.2

28. Removal of implantation mask (time: 10 min)

step	gas 1 O_2 (ml/min)	gas 2 N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	120:00
4	0	500	0	01:00

29. Standard wafer cleaning (time: 30 min)

30. Cleaning of annealing furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	30
1100 - 800	-7.5	N_2	2	40

31. Removal of lattice damage (time: 120 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800	-	N_2	4	30

32. Photolithography of implantation mask (mask SC) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
3000 rpm 20 s	1	6.0	1	45	**30**

33. Implantation of substrate contact regions

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	mass (amu)	2nd magnet (A)
BF_2^+	$2.0 \cdot 10^{15}$	1067	70	49 (48.81)	10.7

34. Removal of implantation mask (time: 10 min)

step	gas 1 O_2 (ml/min)	gas 2 N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	120:00
4	0	500	0	01:00

35. Standard wafer cleaning (time: 30 min)

36. Cleaning of annealing furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	30
1100 - 800	-7.5	N_2	2	40

37. Removal of lattice damage (time: 120 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800	-	N_2	4	30

38. Implantation of gettering dopant (time: 120 min) **BACKSIDE OF WAFER**

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	mass (amu)	2nd magnet (A)
P^+	$8.0 \cdot 10^{15}$	4268	100	31 (30.97)	10.0

39. Standard wafer cleaning (time: 30 min)

40. Cleaning of annealing furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	4	25
1100	-	O_2 / $C_2H_2Cl_2$	2	35
1100 - 800	-7.5	N_2	2	40

41. Dopant activation / gettering (time: 120 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
550	-	N_2	4	60
800 - 900	10	N_2	4	10
900	-	N_2	4	59
900	-	O_2	4	1
900 - 600	-2	N_2	4	150

Comments: cooldown to 550 °C requires extra time

42. Standard wafer cleaning (time: 30 min)

43. Photolithography of gate area (mask GA) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	4.5	1	45	15

44. Etching of sacrificial oxide (time: 10 min) **LIGHT OFF**

	SiO_2 etch	etch rate (nm/min)	etch time
1	1% HF	3 - 4	4 min
2	0.3% HF + 0.37% HCl	slow	6 min + 2 min overetch

Comments: backside dummy wafer: 10 min step 2

45. Resist removal and cleaning (time: 30 min) **NEW CHEMICALS**

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 µS
4	boiling HNO_3 69% 110 °C	10 min
5	rinsing DI water	until conductivity < 0.1 µS
6	spin dry	

46. Cleaning of oxidation furnace (time: 120 min) **WITHOUT WAFERS**

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 850	10	O_2	2	5
850 - 1100	10	O_2 / $C_2H_2Cl_2$	2	25
1100	-	O_2 / $C_2H_2Cl_2$	2	30
1100 - 800	-7.5	N_2	2	40

47. Growth of 10 nm oxide (time: 90 min)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	time (min)
800 - 950	10	O_2 / $C_2H_2Cl_2$	2	15
950	-	N_2	2	10
950 - 800	-7.5	N_2	2	20

48. Etch oxide (time: 30 min)

solution	time (min)
0.3% HF + 0.37% HCl	until reference area hydrophobic

Comments: 12 minutes

49. ALD of AlO layer

50. ALD of TiN layer

51. Photolithography of gate cover (mask GC) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	4.5	1	45	15

52. Etching of gate cover (time: 2 min)

etchant	temperature (°C)	etch rate (nm/min)	etch time (s)
hydrogen peroxide H_2O_2	RT	?	10 min

53. Resist removal and cleaning (time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 µS
4	spin dry	

Comments: no boiling HNO_3!

54. Surface states anneal (time: 15 min) **OPTIONAL**

temperature	ambient	time
400 °C	$N_2 + H_2O$	60 min

55. Photolithography of contact holes (mask CO) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	4.5	1	45	15

56. Etching contact holes (gate oxide + pad oxide) (time: 2 min) **LIGHT OFF**

SiO_2 etch	etch rate (nm/min)	etch time (min:s)
1 % HF		4:30

Comments: ultrasonic surface wetting

57. Resist removal (time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 µS
4	spin dry	

58. Metallization (time: 60 min)

	Ar flow (sccm)	pressure (mTorr)	power (W)	V_{DC} (V)	sputter rate (nm/min)	sputter time (min)	thickness (nm)
TiW	200	10.0	500	343	0.78	1:30	70
Al	210	10.0	7000	425	13.3	1:15	1000

59. Photolithography of interconnect (mask IN) (time: 30 min)

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	4.5	1	45	15

60. Etching of interconnect (time: 2 min)

etchant	temperature (°C)	etch rate (nm/min)	etch time (min)
phosphoric acid H_3PO_4 (+ $CH_3COOH + HNO_3$)	40	200	4
hydrogen peroxide H_2O_2	RT	?	10

Comments: until clear pattern

61. Resist removal and cleaning (time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	spin dry	

Comments: boiling HNO_3 will remove the aluminum!

62. Sintering (time: 15 min) **OPTIONAL**

temperature	ambient	time
400 °C	$N_2 + H_2O$	10 min

List of symbols

The following table contains all symbols used in this dissertation with a short description and their commonly used unit.

symbol	description	(value) [unit]
a	screening length	[Å]
a_0	Bohr radius	0.529177 [Å]
c	speed of light	299792458 [m s^{-1}]
d	distance (between lattice planes)	[Å]
e	electron charge	1 [eV]
f	(scattering) factor	[ ]
f	frequency	[Hz]
g_{ds}	transconductance	[S]
g_{ox}	oxide conductance	[S]
h	Planck's constant	6.62608·10^{-34} [J s]
$\hbar$	Planck's constant (reduced)	1.05457·10^{-34} [J s]
$\boldsymbol{k}$	wave vector	
l	length	[mm]
l_e	effective range (of photoelectrons)	[nm]
m	free electron mass	9.10939·10^{-31} [kg]
m_{ox}	effective electron mass in oxide	[kg]
m^*	relative effective electron mass	[ ]
n	integer value	$\mathbb{N}$ [ ]
n	refractive index	[ ]
p	pressure	[mbar]
$\boldsymbol{p}$	momentum	
p	ALD cycle (integer)	$\mathbb{N}$ [ ]
q	elementary charge	1.602177·10^{-19} [C]
r	radius	[Å]
$\boldsymbol{s}$	scattering vector	
t	time	[s]
t_{ox}	physical oxide thickness	[nm]
$\boldsymbol{u}$	momentum transfer vector	
w	width	[mm]

symbol	description	(value) [unit]
x_j	junction depth	[nm]
A	area	[cm^2]
A	amplitude	[ ]
C_{ox}	oxide capacitance	[F cm^{-2}]
CET	capacitance equivalent thickness	[nm]
D	diffusion constant	[cm^2 s^{-1}]
D	displacement	[C m^{-2}]
E_{ox}	electrical field in the oxide	[V cm^{-1}]
E_{vacuum}	vacuum energy level	[eV]
E_A	activation energy	[eV]
E_C	conduction band energy level	[eV]
E_F	Fermi energy level	[eV]
E_{Fi}	intrinsic Fermi energy level	[eV]
E_G	bandgap	[eV]
E_V	valence band energy level	[eV]
EOT	equivalent oxide thickness	[nm]
G	Gibbs energy	[J]
H	enthalpy	[J]
I	intensity	[ ]
I_D	drain current	[A]
I_{DT}	direct tunneling current	[A cm^{-2}]
I_{FN}	Fowler-Nordheim tunneling current	[A cm^{-2}]
L	channel length	[µm]
N_A	Avogadro's constant	$6.02214 \cdot 10^{23}$ mol^{-1}
N_A	dopant concentration	[cm^{-3}]
P	polarization	
Q	quality factor	[ ]
Q_s	substrate charge	C cm^{-2}
R	gas constant	8.3145 J mol^{-1} K^{-1}
R	surface roughness	[ ]
R_s	series resistance	[Ω]
S	surface fraction	[ ]
S	entropy	[J K^{-1}]
T	temperature	[K] or [°C]
V	volume	[cm^3]
V	voltage	[V]
V_{fb}	flatband voltage	[V]
V_g	gate voltage	[V]
V_{ox}	oxide potential	[V]
V_t	threshold voltage	[V]
W	channel width	[µm]
Z	atom number	[ ]
Z	impedance	[Ω]
α	scaling factor	[ ]
β	gain factor	[V^2 A^{-1}
δ	loss angle	[°]
ε'	permittivity (real part)	[F cm^{-1}]
ε''	permittivity (imaginary part)	[F cm^{-1}]
ε_0	permittivity of free space	$8.8542 \cdot 10^{-14}$ [F cm^{-1}]
ε_∞	refractive index based permittivity	[ ]

symbol	description	(value) [unit]
θ	diffraction angle	[°]
ϑ	mobility lowering factor	[ ]
κ	relative dielectric constant	[ ]
λ	(electron) wavelength	[m^{-1}]
μ_0	low-field mobility	[cm^2 $(V\ s)^{-1}$]
μ_{eff}	effective electron mobility	[cm^2 $(V\ s)^{-1}$]
ρ	charge density	[]
$\rho_{\square,ch}$	sheet resistivity channel	[Ω/□]
$\rho_{\square,g}$	sheet resistivity gate	[Ω/□]
$\rho_{\square,w}$	sheet resistivity well	[Ω/□]
τ	layer completion time	[s]
ϕ / φ	angle (of incidence)	[°]
φ_{ms}	metal-semiconductor workfunction	[V]
χ	electron affinity	[V]
χ_e	electronic susceptibility	[ ]
ΔE_C	conduction band offset	[eV]
Θ	layer coverage	[ ]
Φ_{ox}	oxide potential	[V]
Φ_B	barrier height	[V]
Φ_M	metal workfunction	[V]

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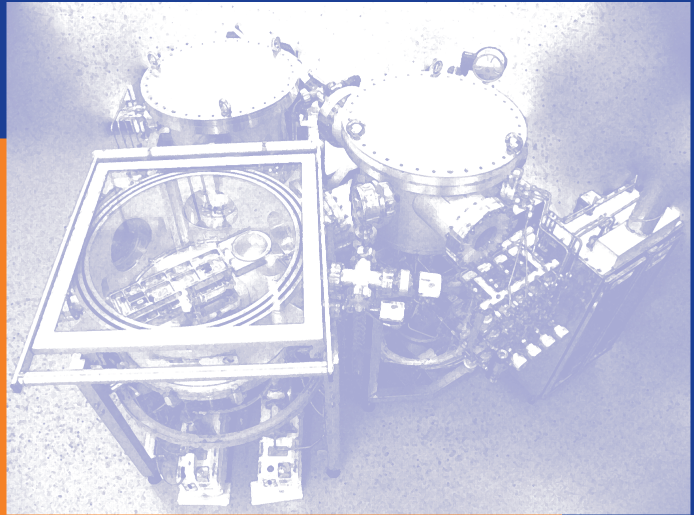

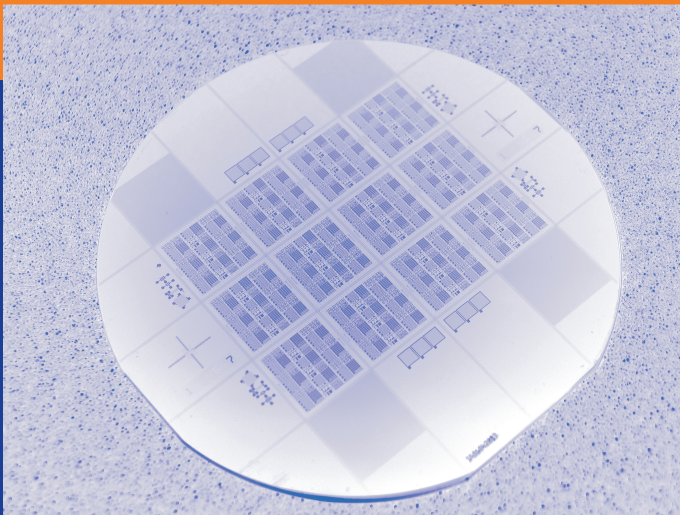

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